ADFP Cloud 2.0

Full-custom 設計使用者手冊

2024.11.18 Version 1

Author

莊勝傑、施品辰、蕭邦原

Editor

賴林鴻

目錄

1. ADFP Cloud 2.0 PDK 下載與安裝

1.1 拷貝製程資料夾

目標資料夾: /ADFP/Executable_Package/Collaterals/Tech/iPDK/N16ADFP_iPDK/

[~]$ cd ~

[~]$ mkdir ADFP

[~]$ cd ADFP

[~/ADFP]$ cp -r /ADFP/Executable_Package/Collaterals/Tech/iPDK/N16ADFP_iPDK/ .

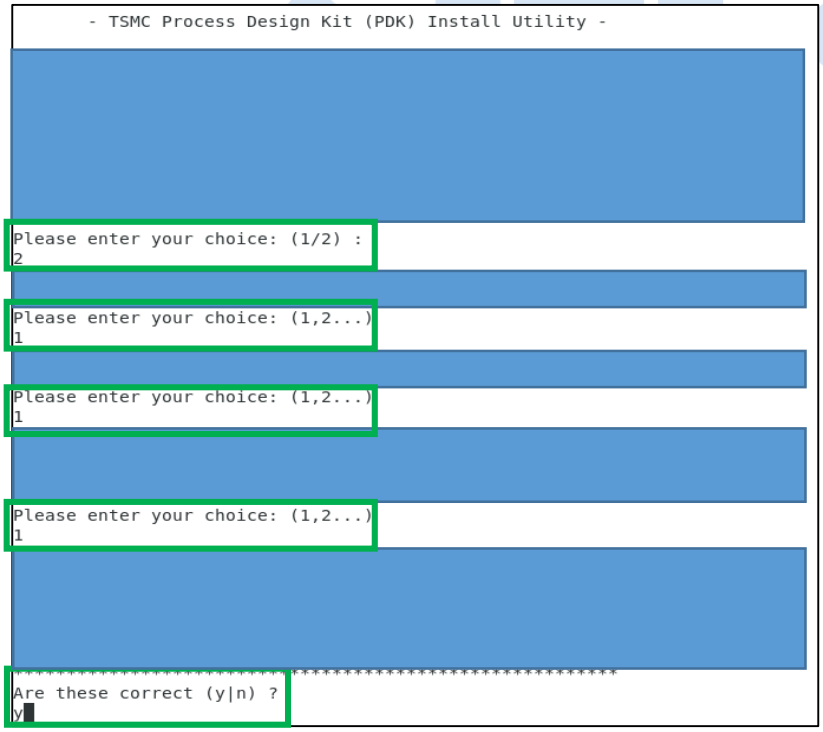
```
DING! vlsi_labTA01@cad11[~]$ cd ~
15:01 vlsi_labTA01@cad11[~]$ mkdir ADFP
15:02 vlsi_labTA01@cad11[~/ADFP]$ cp -r /ADFP/Executable_Package/Collaterals/Tech/iPDK/N16ADFP_iPDK/ .
15:04 vlsi_labTA01@cad11[~/ADFP]$ cd N16ADFP_iPDK/
15:09 vlsi_labTA01@cad11[~/ADFP/N16ADFP_iPDK]$ ./p
pdkInstall.cfg* pdkInstall.pl*
15:09 vlsi_labTA01@cad11[~/ADFP/N16ADFP_iPDK]$ ./pdkInstall.pl
```

1.2 安裝 PDK (必要步驟)

於該資料夾中執行 ./pdkInstall.pl，並依序輸入 「2, 1, 1, 1, y」

[~/ADFP]$ cd N16ADFP_iPDK

[~/ADFP/N16ADFP_iPDK]$ ./pdkInstall.pl



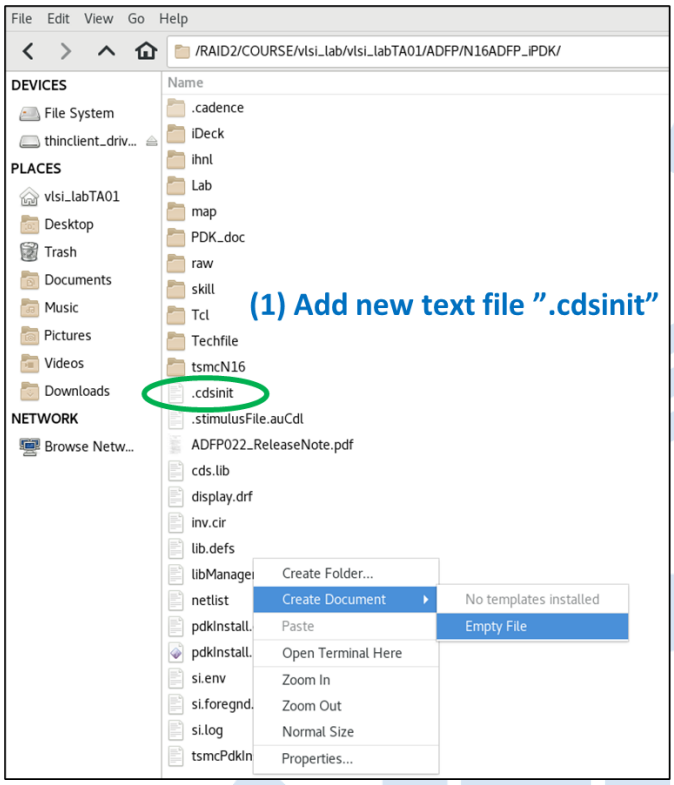
1.3 確認是否正確完成安裝

出現以下畫面代表成功安裝

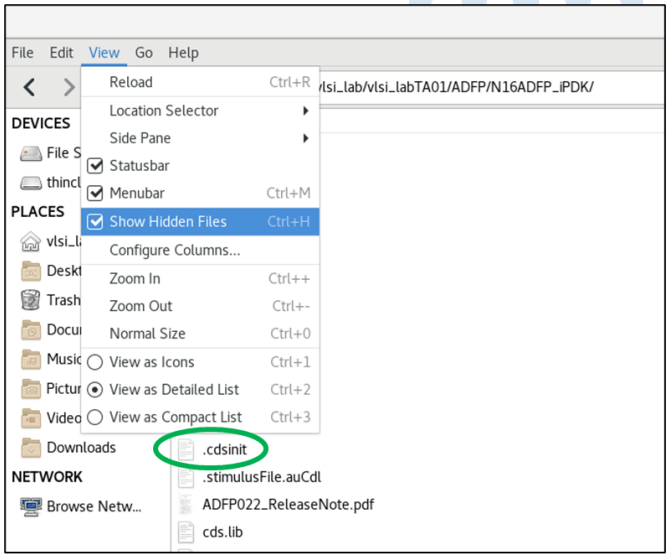
```
*Info: PDK installation completed.
15:13 vlsi_labTA01@cad11[~/ADFP/N16ADFP_iPDK]$
```

1.4 創建並修改.cdsinit 檔案

(1) 在 N16ADFP_iPDK 資料中，新增「.cdsinit」檔案



(2) 將隱藏的檔案顯示



(2) Show hidden file to find ".cdsinit"

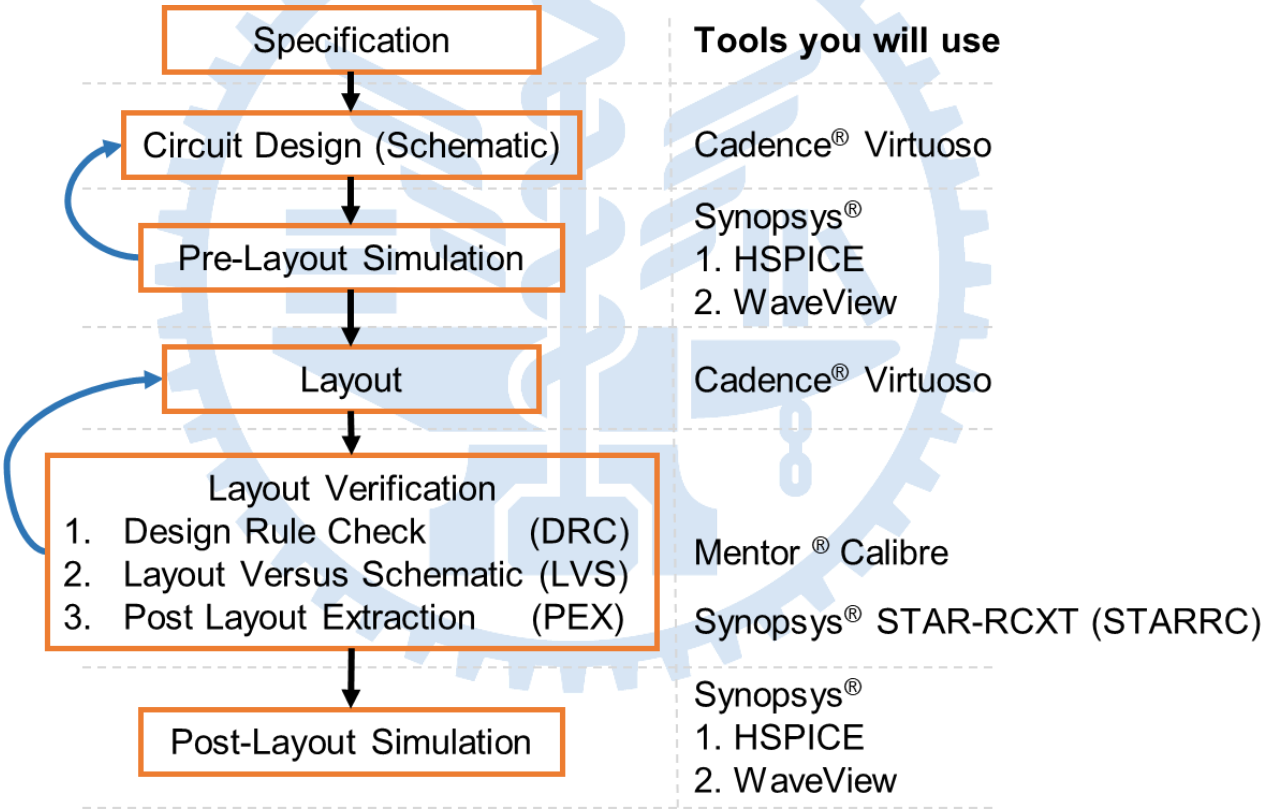
(3) 打開檔案並加入以下文字，這會讓 Calibre 加入 Virtuoso 畫面中

```
;Set Calibre Path

load(strcat(getShellEnvVar("MGC_HOME") "/lib/calibre.OA.skl"))
```

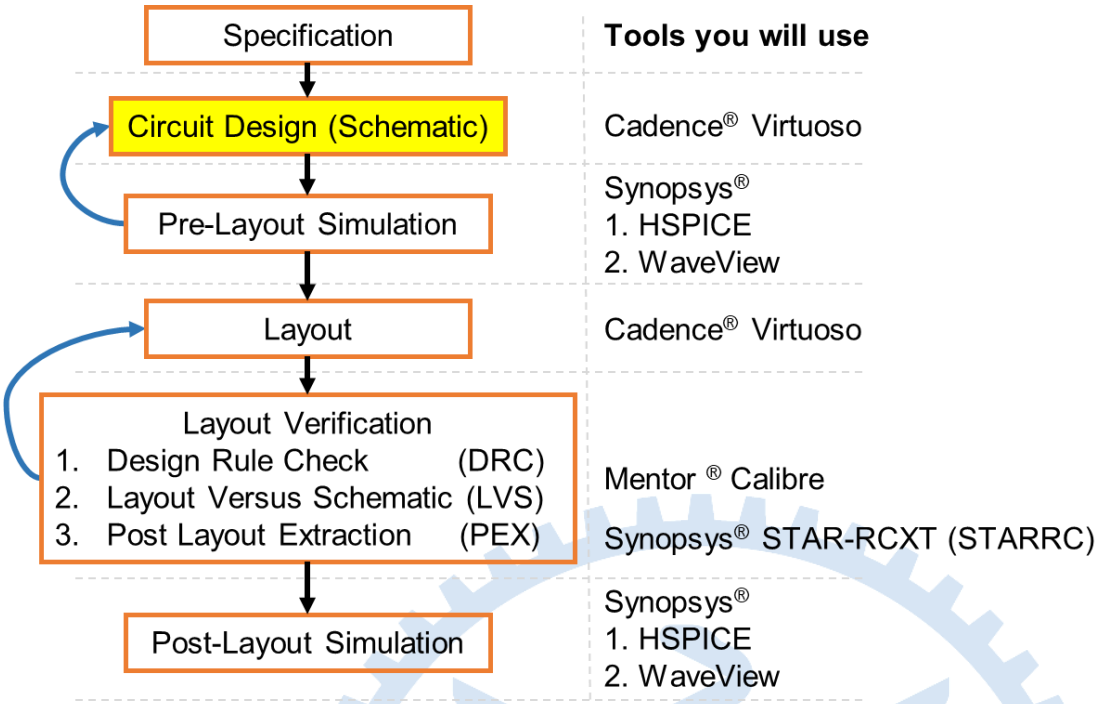
(3) Add text into ".cdsinit"
This step is to add Calibre Interface into Virtuoso

1.5 安裝完成^w^

1.6 在這個範例教程，將會使用以下 EDA 工具作為教學



2. Circuit Design (Schematic)



2.1 裝載所需的 EDA Tool 環境

打開 Terminal 輸入以下指令

[~/ADFP/N16ADFP_iPDK]$ yes

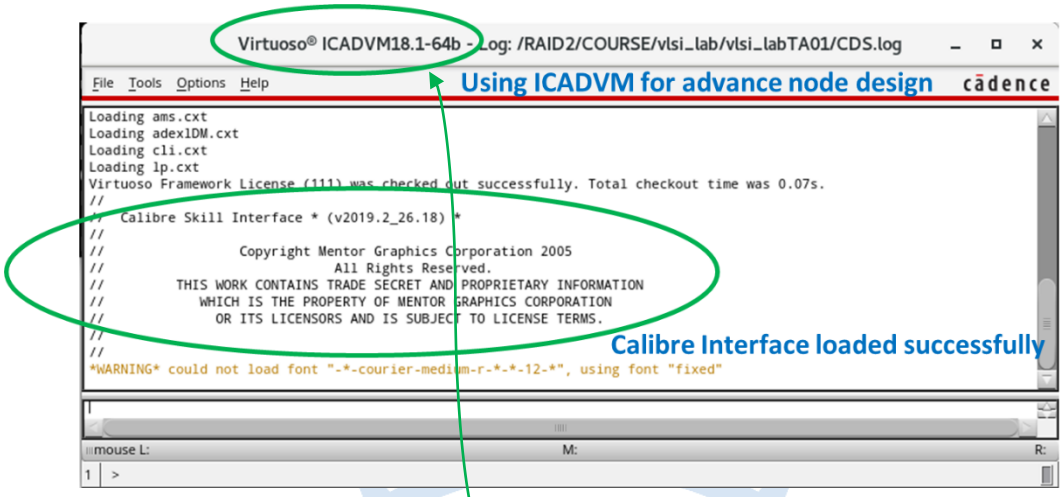
[~/ADFP/N16ADFP_iPDK]$ source /ADFP/cshrc/ADFP_FC_Tool.cshrc

```
set ICADVM version: ICADVM_18.10.130/ (default)
set QUANTUS version: QUANTUS_21.11.000/ (default)
set calibre version : aoi_cal_2019.2_26.18/
set hspice version: 2020.03-sp2-2/ (default)
lsof: WARNING: can't stat() fuse.gvfsd-fuse file system /run/user/0/gvfs
      Output information may be incomplete.
lsof: WARNING: can't stat() fuse.gvfsd-fuse file system /run/user/1001/gvfs
      Output information may be incomplete.
lsof: WARNING: can't stat() fuse.gvfsd-fuse file system /run/user/1125/gvfs
      Output information may be incomplete.
lsof: WARNING: can't stat() fuse.gvfsd-fuse file system /run/user/1202/gvfs
      Output information may be incomplete.
lsof: WARNING: can't stat() fuse.gvfsd-fuse file system /run/user/1143/gvfs
      Output information may be incomplete.
lsof: WARNING: can't stat() fuse.gvfsd-fuse file system /run/user/1209/gvfs
      Output information may be incomplete.
lsof: WARNING: can't stat() fuse.gvfsd-fuse file system /run/user/1212/gvfs
      Output information may be incomplete.
lsof: WARNING: can't stat() fuse.gvfsd-fuse file system /run/user/1208/gvfs
      Output information may be incomplete.
lsof: WARNING: can't stat() fuse.gvfsd-fuse file system /run/user/1210/gvfs
      Output information may be incomplete.
set customexplorer version: 2022.06/ (default)
16:52 vlsi_labTA01@cad11[~/ADFP/N16ADFP_iPDK]$
```

* Do This Step Before Using Any Tool

2.2 打開 Virtuoso 軟體

[~/ADFP/N16ADFP_iPDK]$ virtuoso &

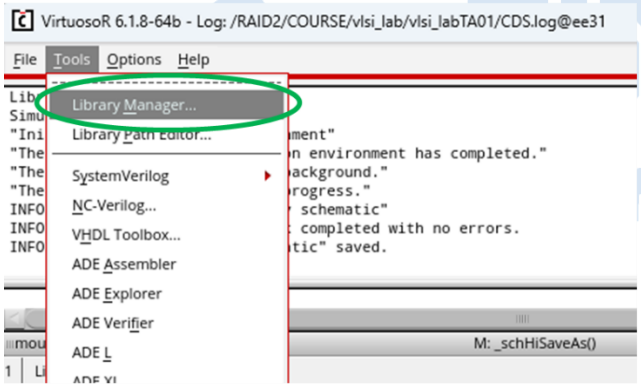


請注意，打開的版本為 ICADVM，而非 IC6。

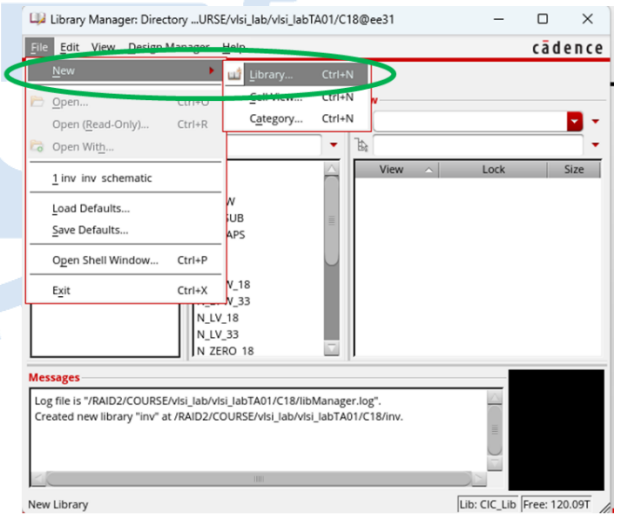
2.3 創建 Library

(1)點選「Tool」→ 「Library Manager」

(2)點選「File」→ 「New」→ 「Library」



(1) Tools -> Library Manager

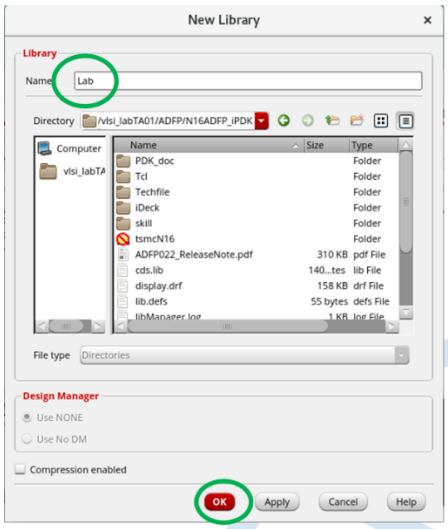


(2) File -> New -> Library

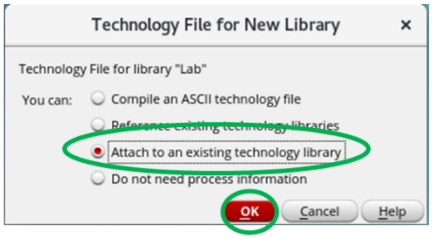
(3)輸入 Library Name (這邊以輸入 “Lab” 示範)

(4)點選「Attach to an existing technology library」→ 「OK」

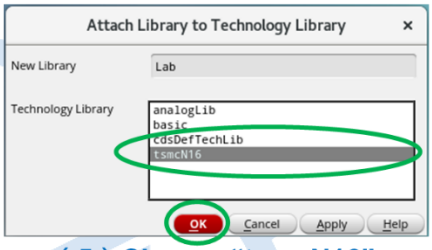
(5)點選「tsmcN16」→ 「OK」



(3) Enter library name “Lab”



(4) Attach to an existing technology library



(5) Choose “tsmcN16”

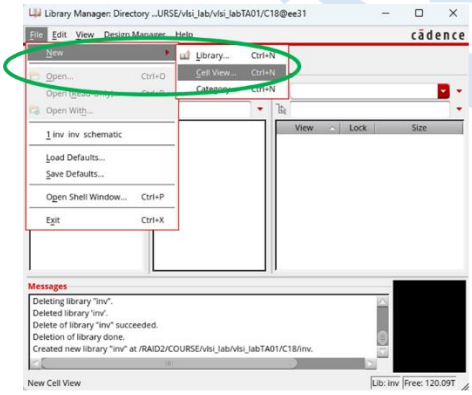
x`

2.4 創建 Schematic

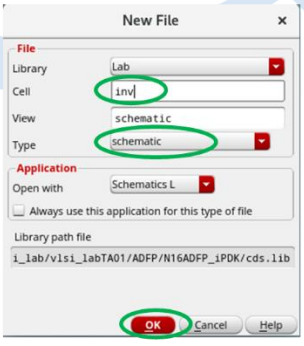
(1)點選「New」→ 「Cell View」

(2)輸入 cell name，點選「schematic」→ 「OK」

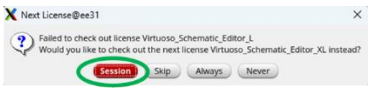
(3)點選「Session」



(1) New -> Cell View



(2) Enter the cell name
Select “schematic”

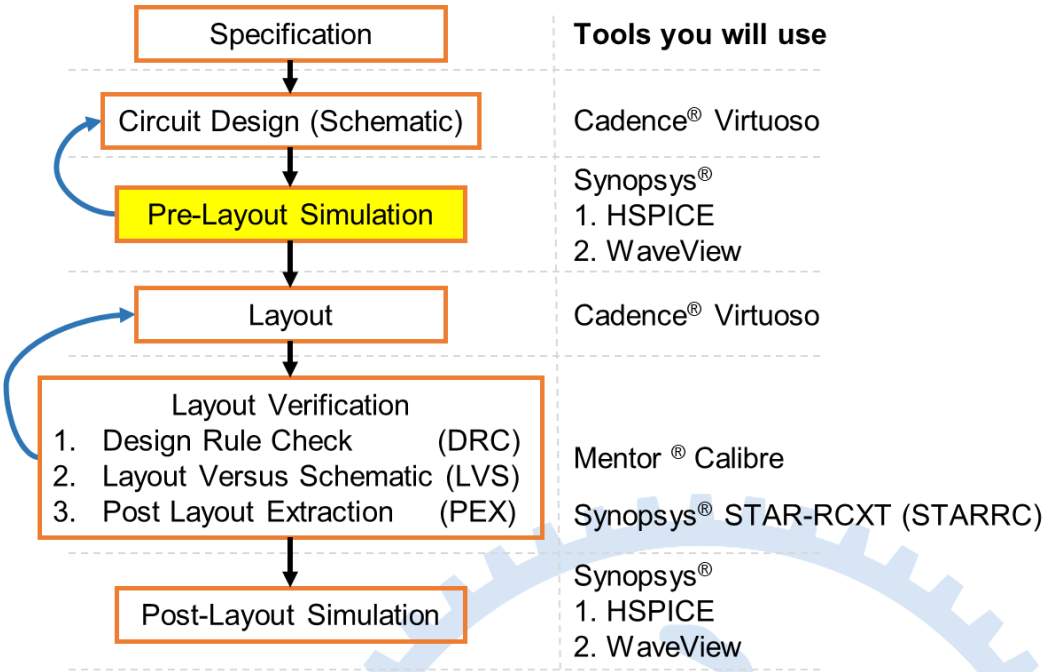


(3) Session

2.5 Create Inverter Schematic / Symbol Design

請根據自行需求繪製 Schematic / Symbol

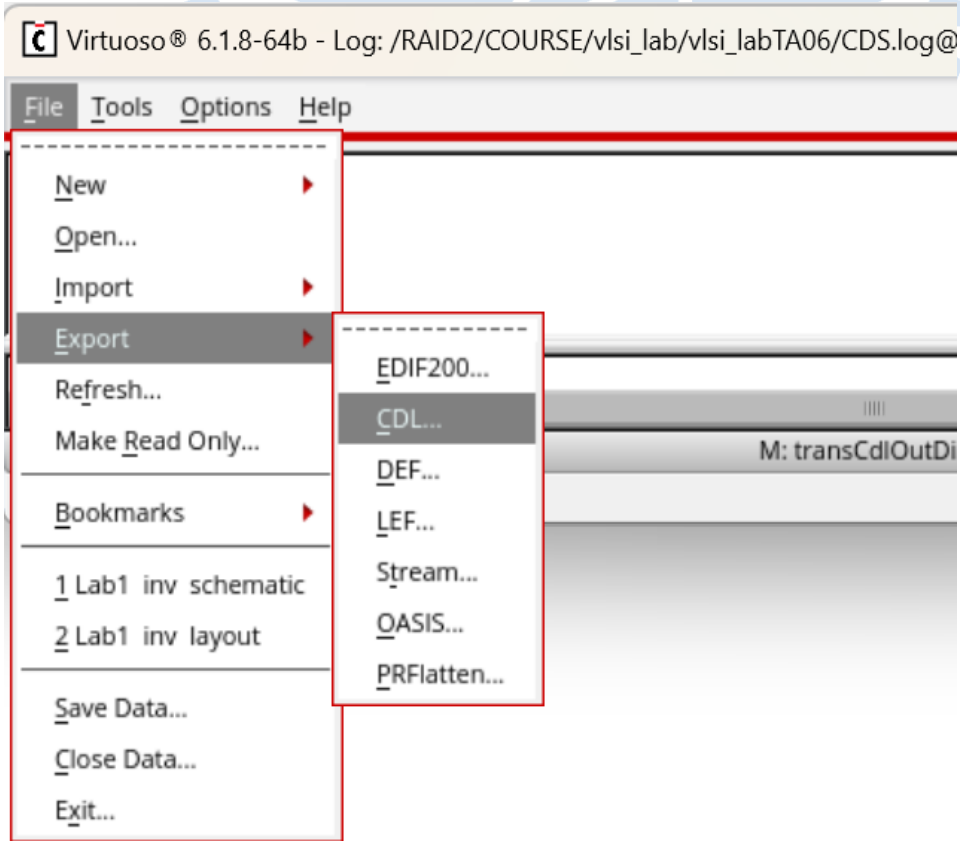
3. Pre-Layout Simulation



3.1 輸出 Spice Netlist

(1)回到 Virtuoso command window

(2)點選「File」→ 「Export」→ 「CDL」

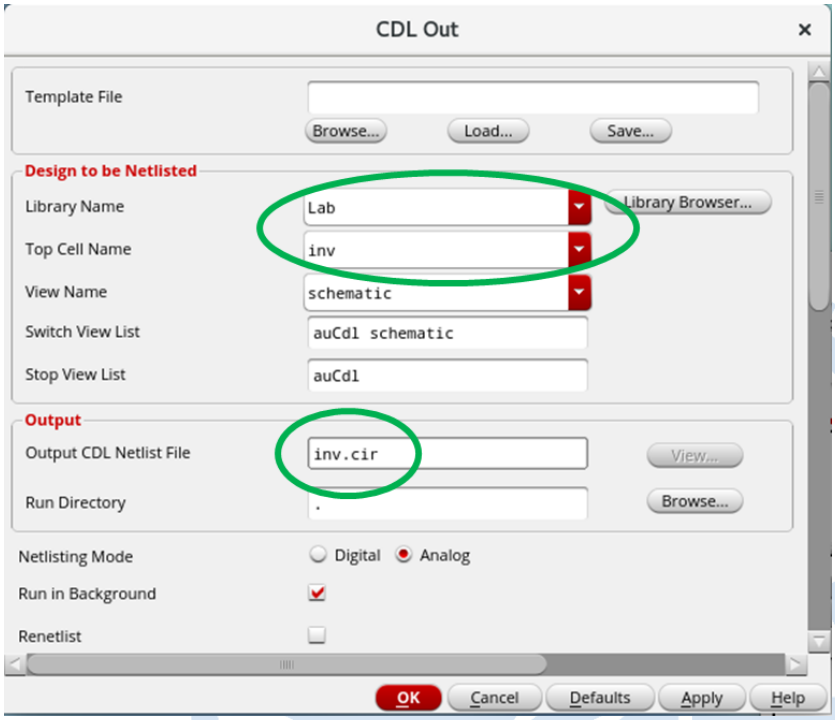


3.2 輸出 Spice Netlist

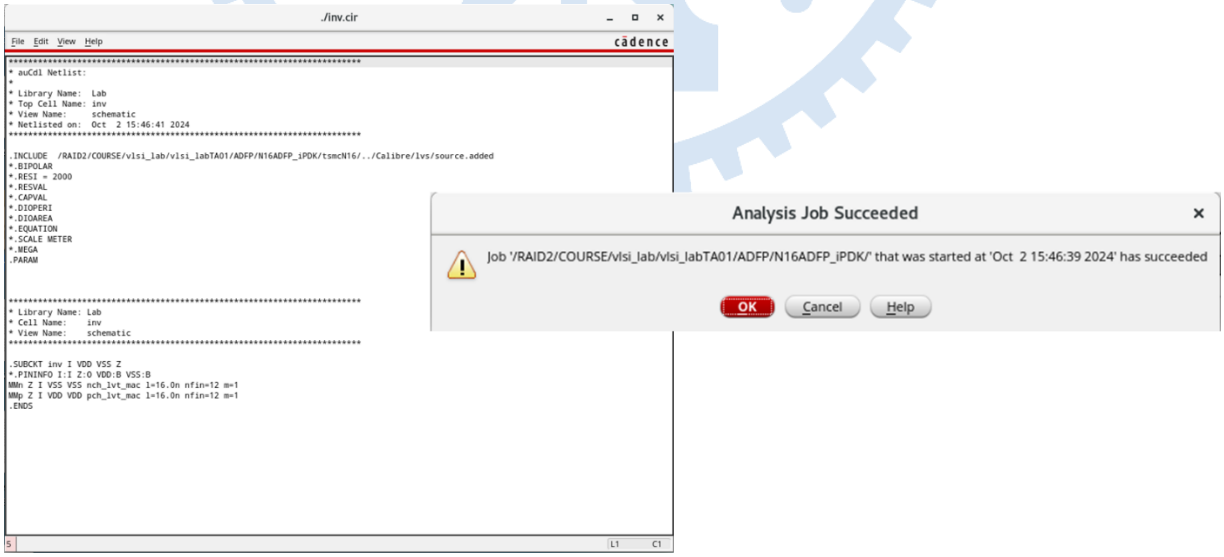
(1)選擇需要輸出德 Library 和 Cell (可使用 Library Browser)

(2)輸入 output netlist 名字，例如 inv.cir

(3)點選「OK」



3.3 點選 OK 成功輸出 Netlist



3.4 複製輸出電路來模擬

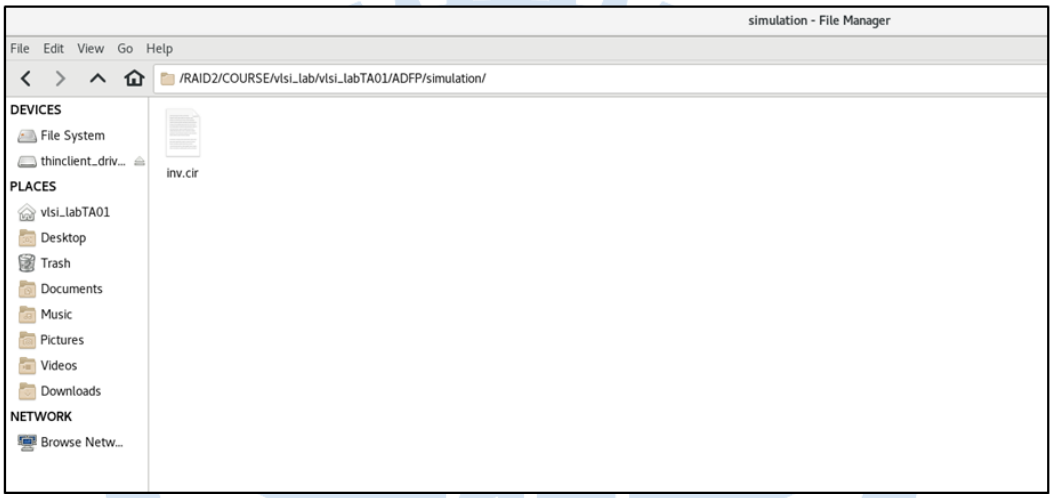
[~]$ cd ~/ADFP

[~/ADFP]$ mkdir simulation

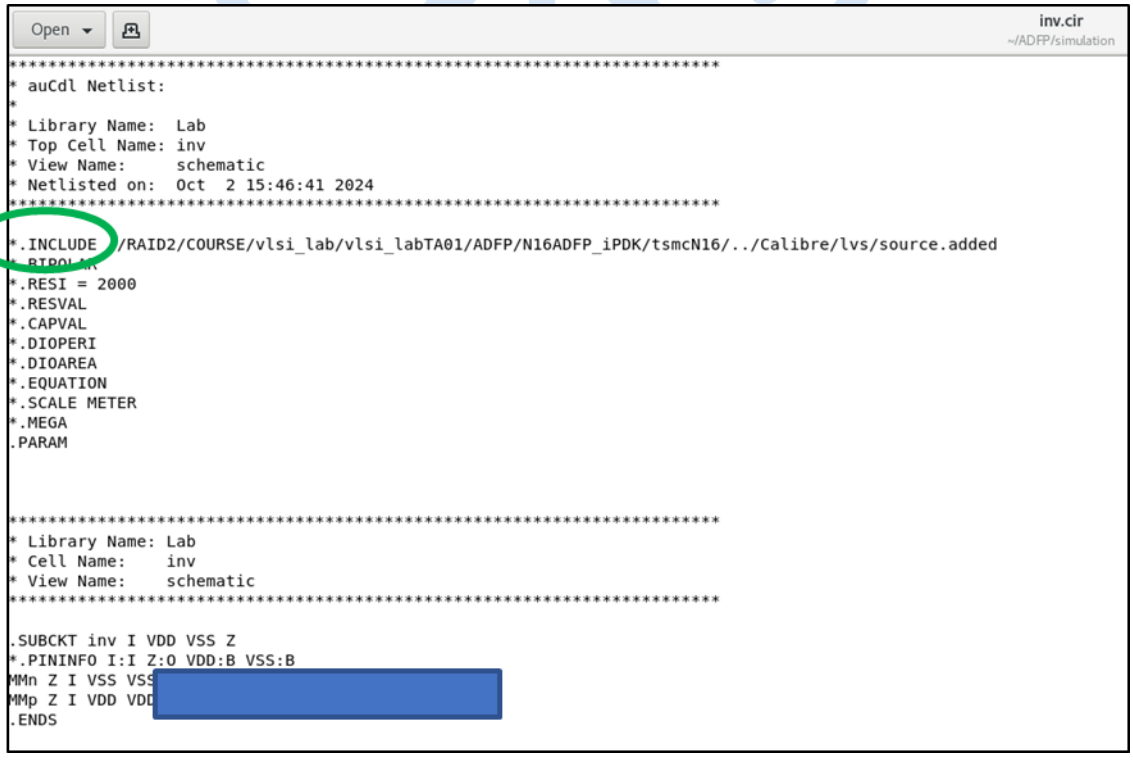
[~/ADFP] $ cd simulation

[~/ADFP/simulation]$ cp ~/ADFP/N16ADFP_iPDK/inv.cir .

```
DING! vlsi_labTA01@cad11[~]$ cd ~/ADFP
16:00 vlsi_labTA01@cad11[~/ADFP]$ mkdir simulation
16:01 vlsi_labTA01@cad11[~/ADFP]$ cd simulation
16:01 vlsi_labTA01@cad11[~/ADFP/simulation]$ cp ~/ADFP/N16ADFP_iPDK/inv.cir .
16:01 vlsi_labTA01@cad11[~/ADFP/simulation]$
```

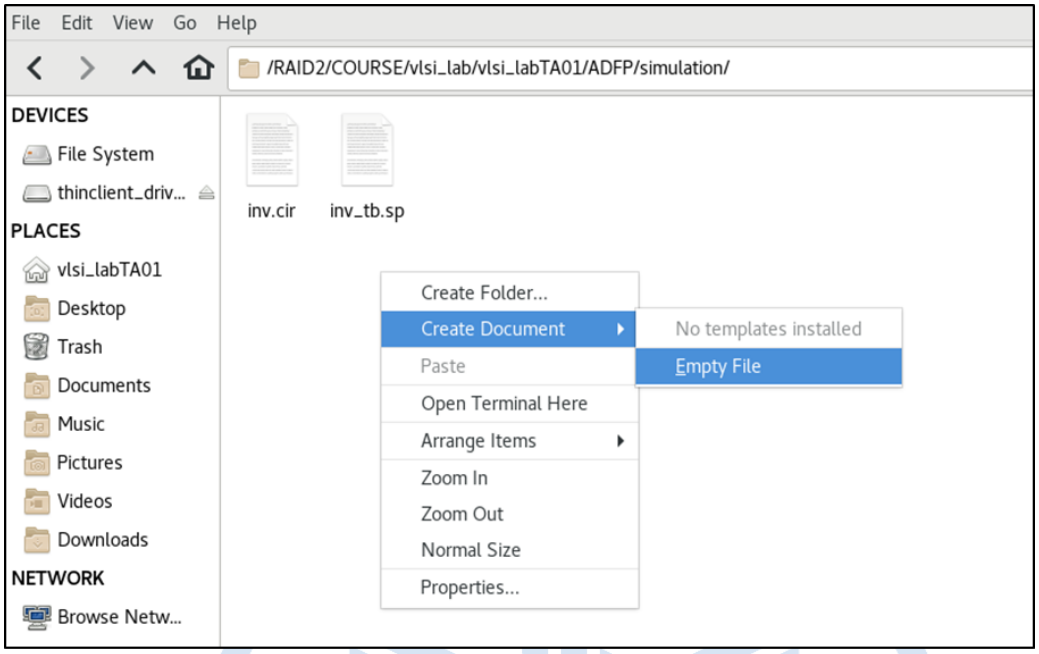


註解以下欄位



3.5 創建模擬環境

(1) 新增一個檔案，這邊以 inv_tb.sp 為範例



(1) Create new text file "inv_tb"

(2)撰寫對應的 Test Bench

Library Path 如下，請記得 include 剛剛匯出的 pre-netlist (這邊是 inv.cir)

Library Path:
/ADFP/Executable_Package/Collaterals/Tech/SPICE/N16ADFP_SPICE_MODEL/n16adfp_spice_model_v1d0_usage.l

(2) Completer Testbench Design

3.6 使用 Hspice 模擬

[~/ADFP/simulation]$ hspice inv_tb.sp

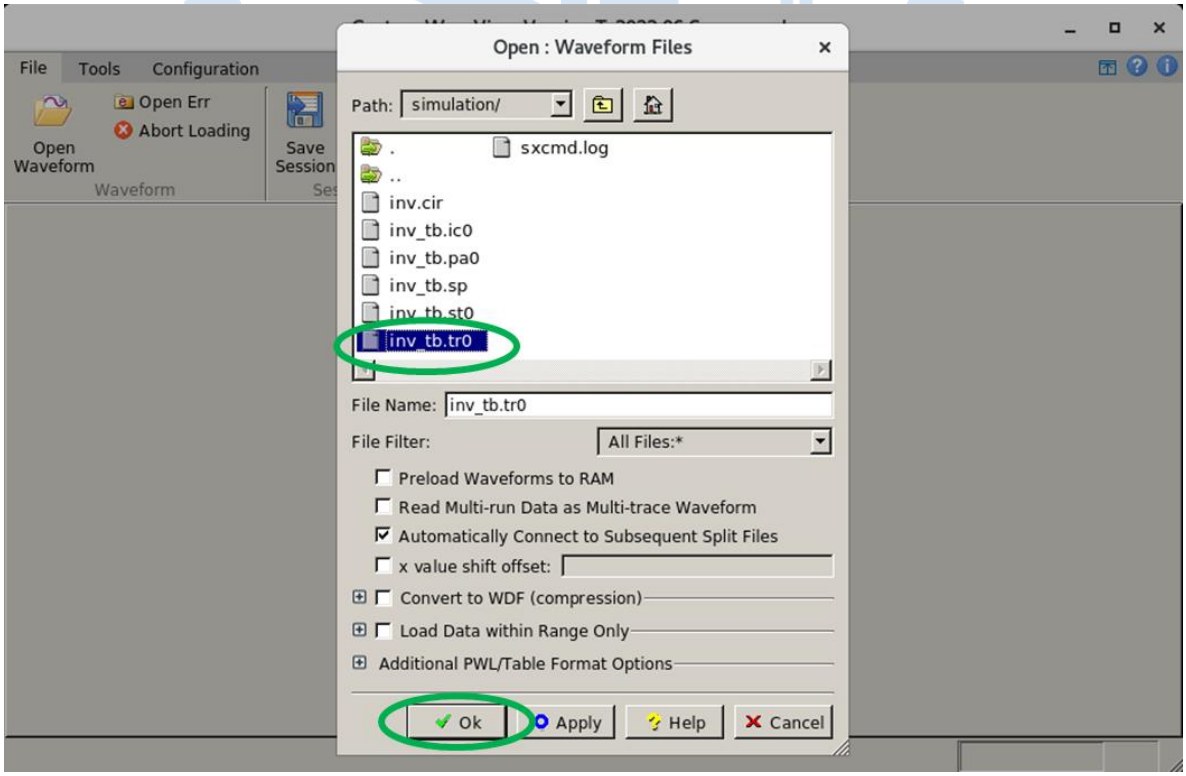
```
******  Runtime Statistics (seconds)  ******

analysis          time    # points   tot. iter  conv.iter
op point          0.01           1           3
transient         0.02       10001        1111         452 rev=        79
readin            0.09
errchk            0.08
setup             0.01
output            0.00


          peak memory used        411.21 megabytes
          total cpu time            0.20 seconds
          total elapsed time        0.36 seconds
          job started at     17:05:39 10/02/2024
          job ended   at     17:05:39 10/02/2024

>info:         ***** hspice job concluded
          job total runtime         0.36 seconds


 lic: Release hspice token(s)
 lic: total license checkout elapse time:        0.15(s)
17:05 vlsi_labTA01@cad11[~/ADFP/simulation]$
```

simulate successfully

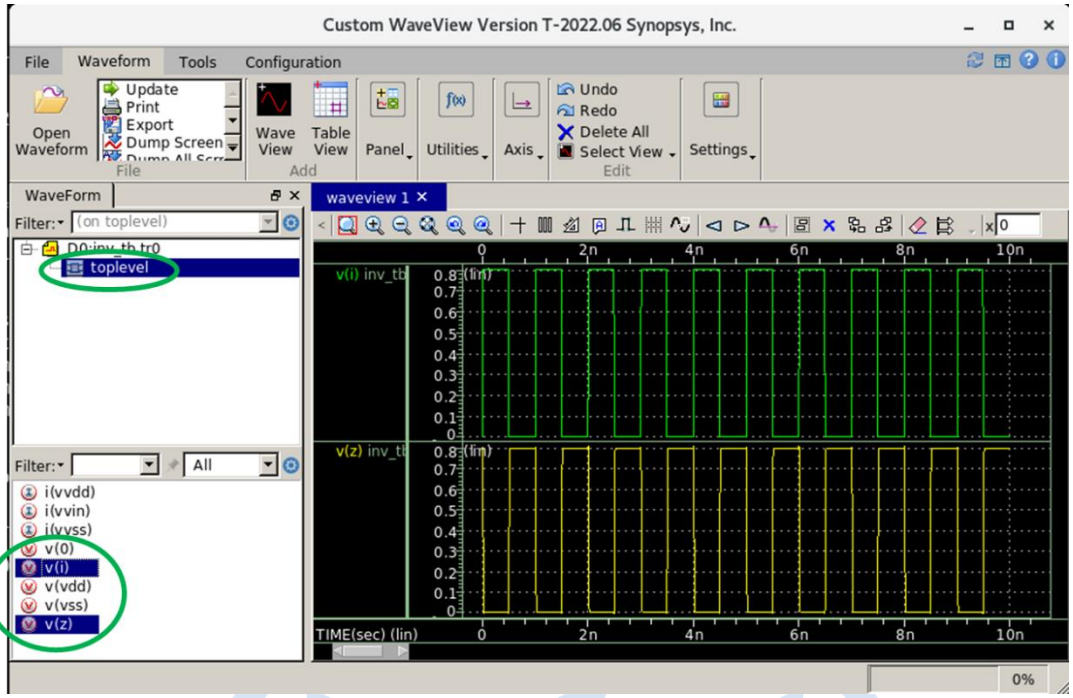
3.7 使用 WaveView 查看波型

[~/ADFP/simulation]$ wv &

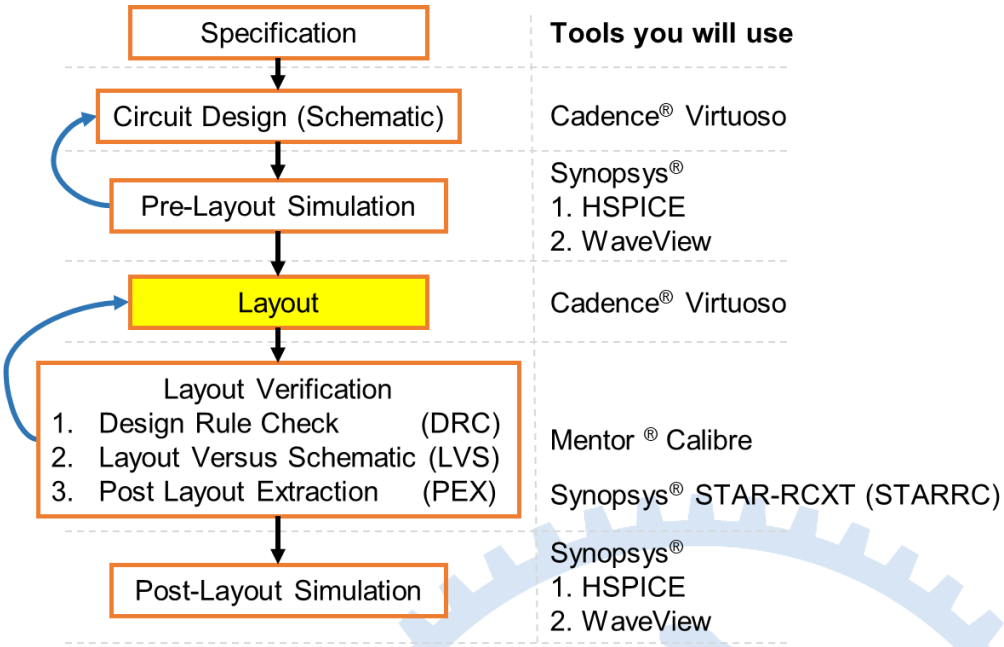
點選波形檔案(通常輸出為 *.tr0)



3.8 點選欲觀察的訊號，即可查看波形



4. Layout

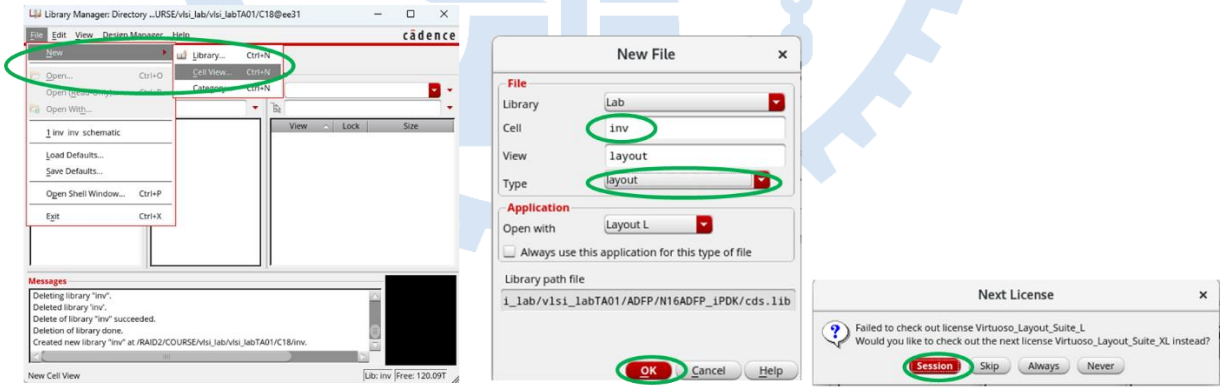


4.1 創建 Layout View

(1)點選「New」→ 「Cell View」

(2)輸入 cell name，點選「layout」→ 「OK」

(3)點選「Session」



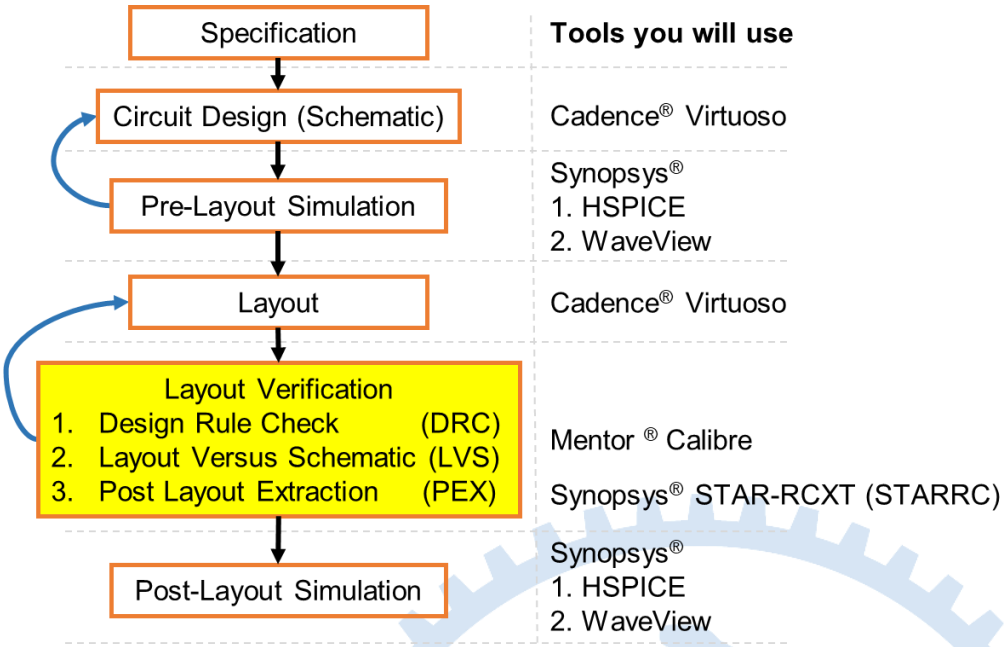
(1) New -> Cell View　　(2) Select "Layout"　　(3) Session

4.2 Create Inverter Layout Design

請根據自行需求創建，可參考相關課程教學文件

COURSE05_VLSILAB_ADFP_layout_tutorial_2024-01-12.pdf

5. Layout Verification – DRC

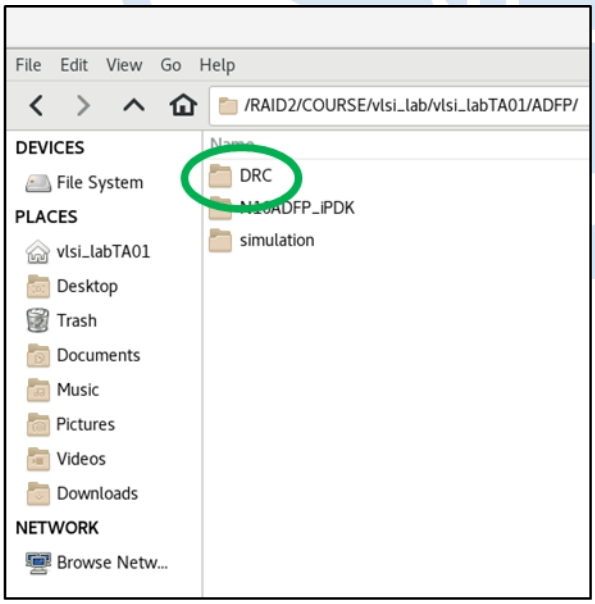


5.1 創建 DRC 資料夾

[~]$ cd ~/ADFP

[~/ADFP]$ mkdir DRC

[~/ADFP]$ cd DRC



(1) Create new folder for DRC

5.2 拷貝 DRC 規則

- **Full-Chip Rule:**

[~/ADFP/DRC]$ cp

/ADFP/Executable_Package/Collaterals/Tech/DRC/N16ADFP_DRC_Calibre/LOGIC_TopMr_DRC/N16ADFP_DRC_Calibre_11M.11_1a.encrypt ./

- **Antenna Rule:**

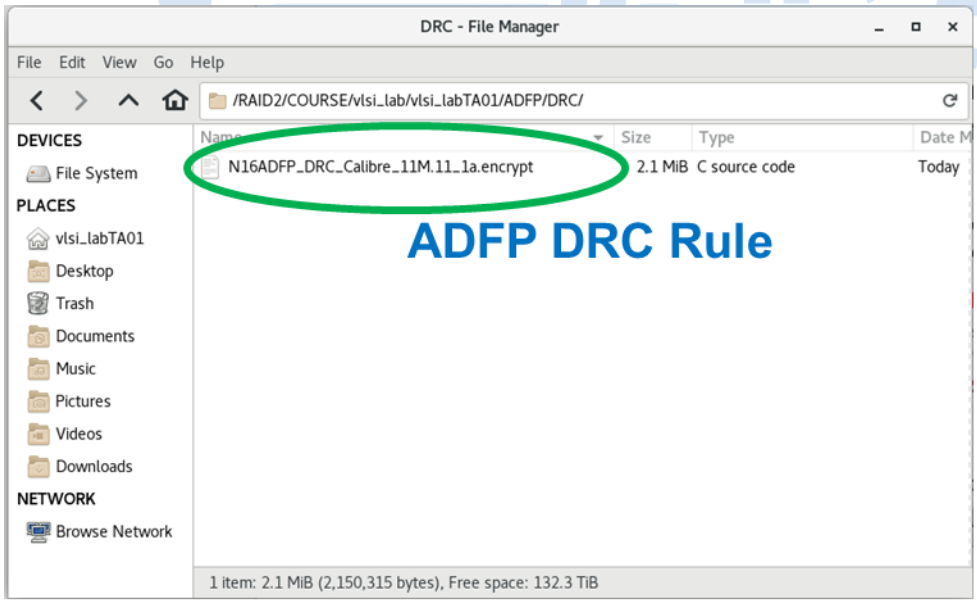
[~/ADFP/DRC]$ cp

/ADFP/Executable_Package/Collaterals/Tech/DRC/N16ADFP_DRC_Calibre/ANTENNA_DRC/N16ADFP_DRC_Calibre_11M_ANT.11_1a.encrypt ./

- **IP-Level Rule:**

[~/ADFP/DRC]$ cp /ADFP/Material/DRC/N16ADFP_DRC_Calibre_11M.11_1a.encrypt ./

一般課程範例建議使用 IP-Level Rule 避免出現一些可在 IP Level 忽略的 DRC，例如: Density Check。



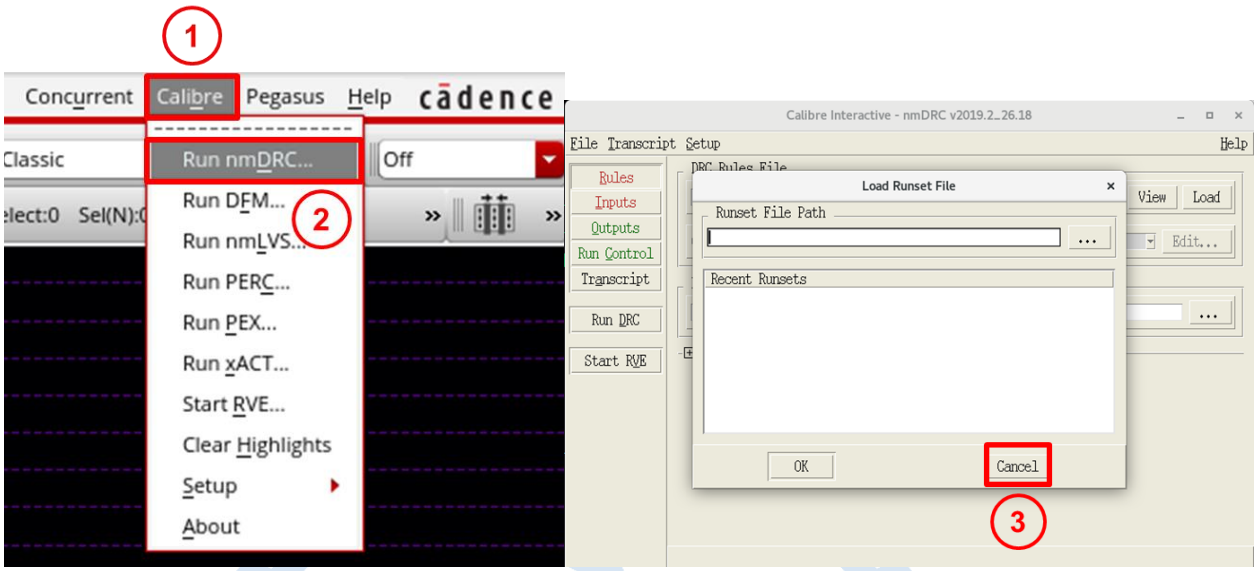
(2) Ensure that DRC rule is copied

如想更了解請參閱家目錄的浮水印文件，有關 DRC Rule 設定:

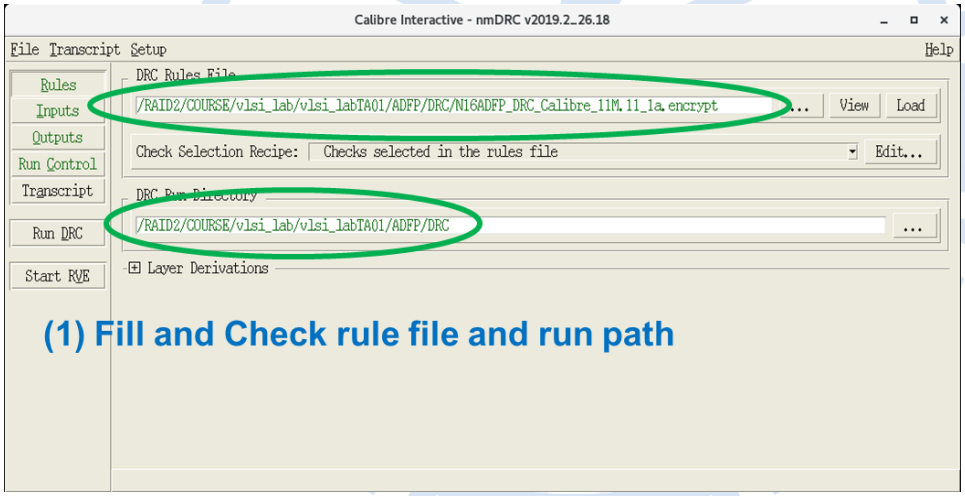
~/Desktop/ADFP_PDF/ADFP040_N16_DRC_Switch_Usage_wmp.pdf

5.3 從 Virtuoso 打開 Calibre

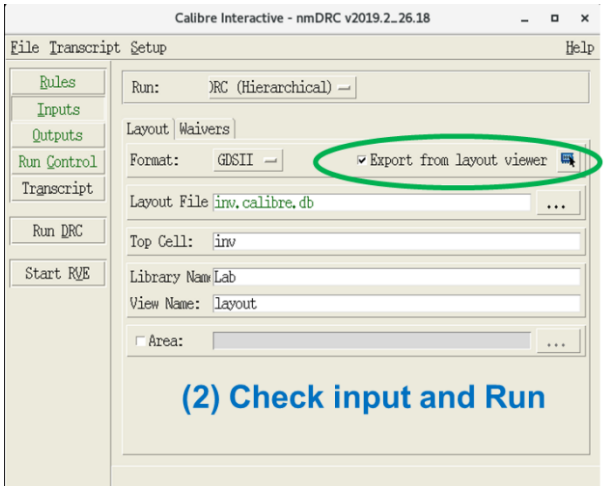
(1)點選「Calibre」→ 「Run nmDRC」→ 「Cancel」



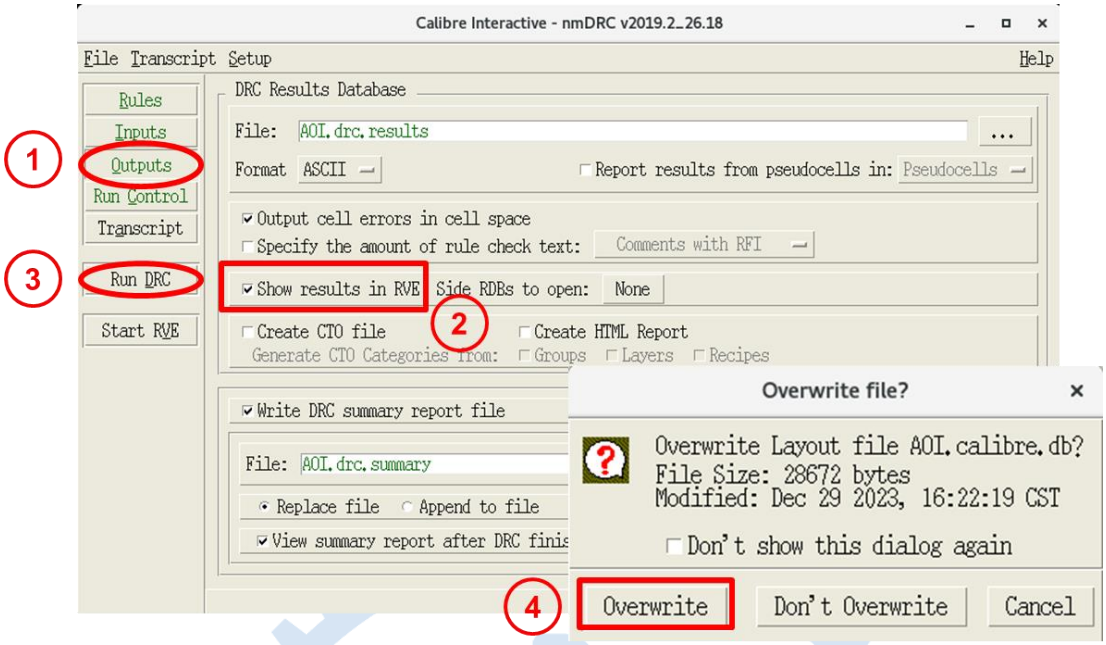
(2)點選「Rules」→ 「Load」→ 「選取剛剛複製過來的 DRC Rule」



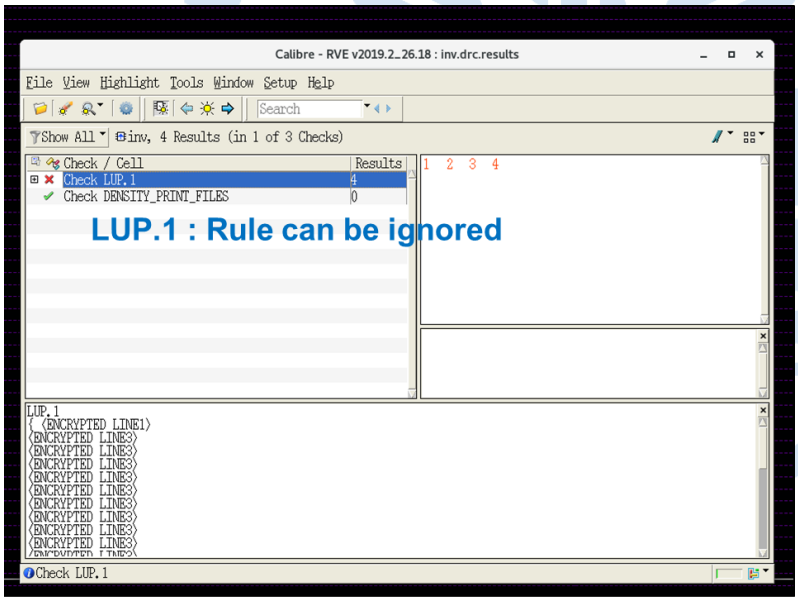
(3)點選「Inputs」→ 勾選「Export from layout viewer」



(4)點選「Outputs」→ 勾選「Show results in RVE」→ 「Run DRC」



5.4 確認 DRC Rule 是哪裡違反



(3) Check DRC Result

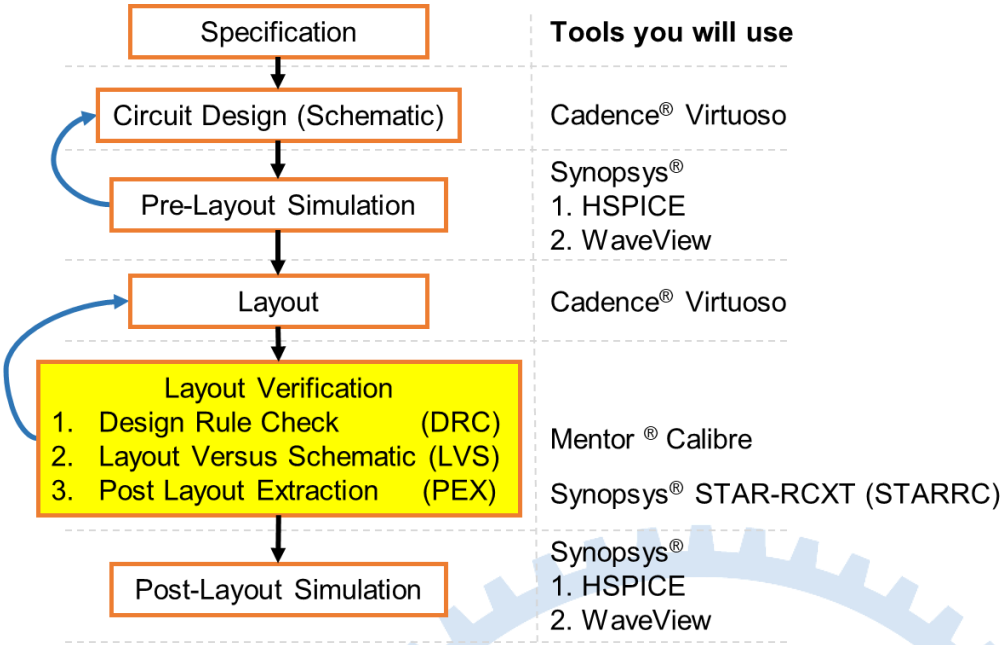
Note: 因 ADFP 的 DRC 有加密，因此違反細節不會顯示在 RVE 當中

如想更了解請參閱家目錄的浮水印文件，有關 DRC Rule 說明:

~/Desktop/ADFP_PDF/ADFP039_N16ADFP_DRM_V1.1_1.pdf

善用 PDF 搜尋功能找到對應的 DRC 規則。

6. Layout Verification – LVS

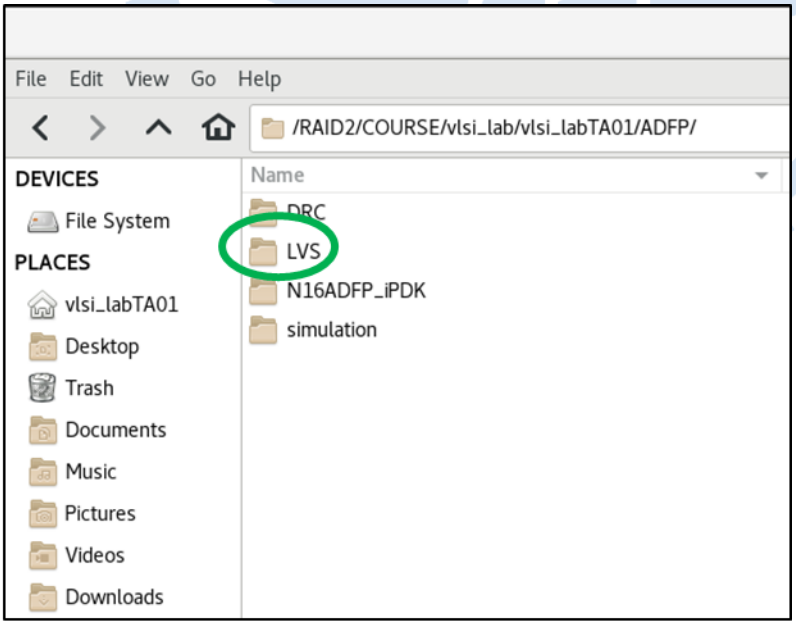


6.1 創建 LVS 資料夾

[~]$ cd ~/ADFP

[~/ADFP]$ mkdir LVS

[~/ADFP]$ cd LVS



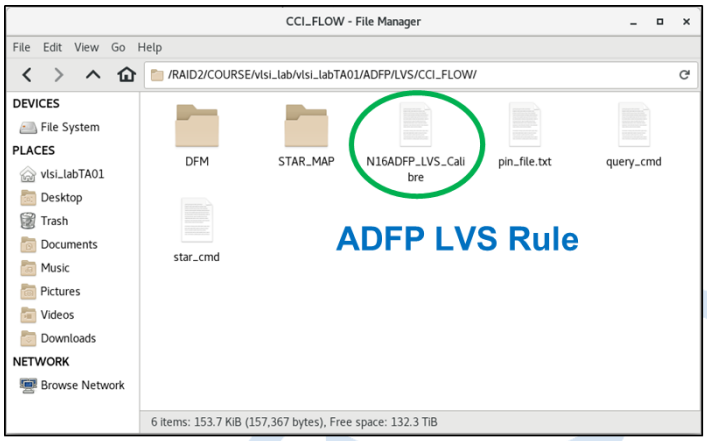
(1) Create new folder for LVS

6.2 拷貝 LVS 規則

LVS Rule:

[~/ADFP/LVS]$ cp -r /ADFP/Material/LVS ./

Rule file name: N16ADFP_LVS_Calibre



(2) Ensure whole directory is copied

如想更了解請參閱家目錄的浮水印文件，有關 LVS Rule 說明:
~/Desktop/ADFP_PDF/

ADFP003_N16_ADFP_Calibre_LVS_BOX_Command_Usage.pdf

ADFP004_N16_ADFP_Calibre_LVS_Deck_Usage.pdf

ADFP005_N16_ADFP_Dummy_Pickup_Checking.pdf

ADFP006_N16_ADFP_ERC_Usage.pdf

ADFP007_N16_ADFP_LOD_Measurement.pdf

ADFP008_N16_ADFP_LVS_Filter_Introduction.pdf

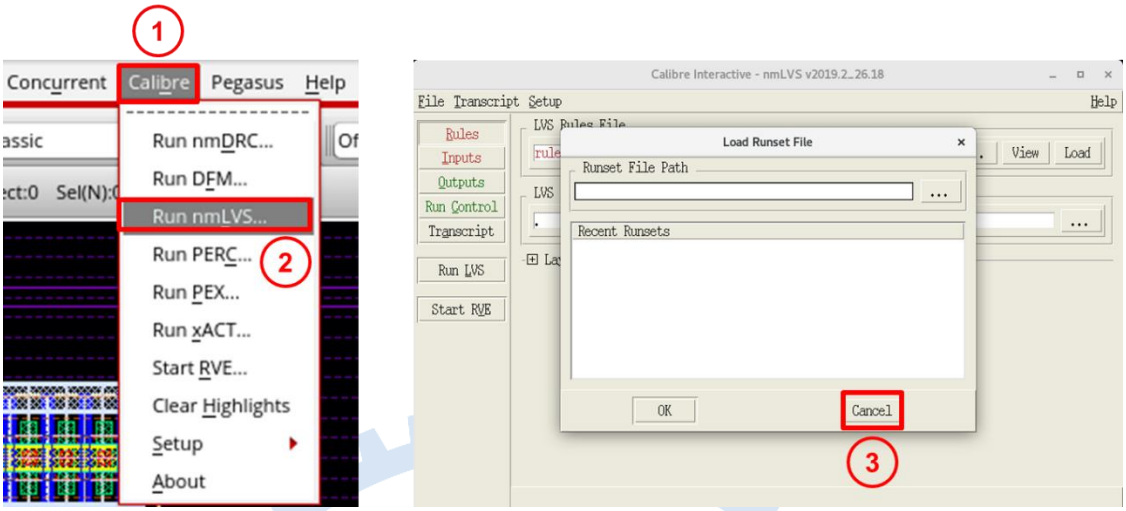
ADFP009_N16_ADFP_NF_MOS_Parallel_Reduction.pdf

ADFP010_N16_ADFP_STD_Filter_Cells.pdf

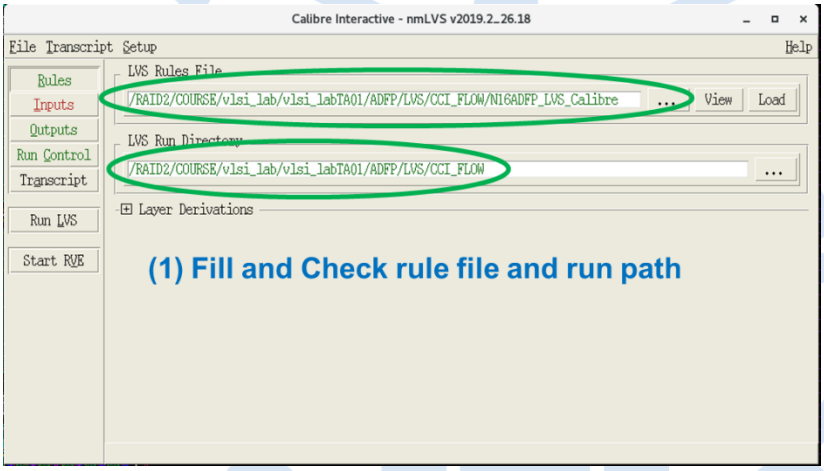
ADFP011_N16_ADFP_Unrecognized_Device.pdf

6.3 從 Virtuoso 打開 Calibre:

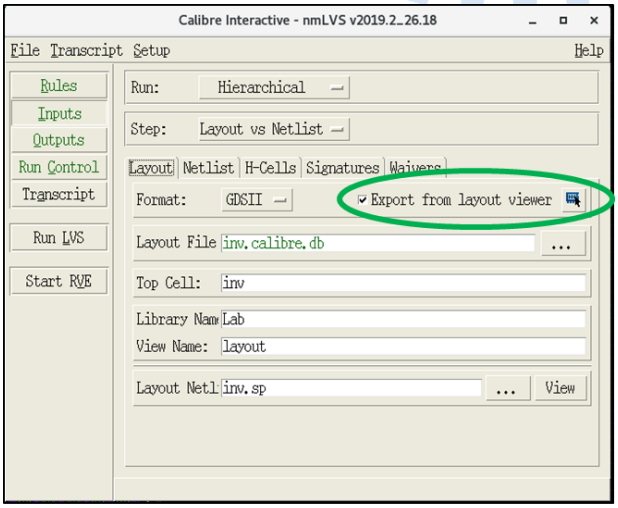
(1)點選「Calibre」→ 「Run nmLVS」→ 「Cancel」



(2)點選「Rules」→「Load」→ 「選取剛剛複製過來的 LVS Rule」



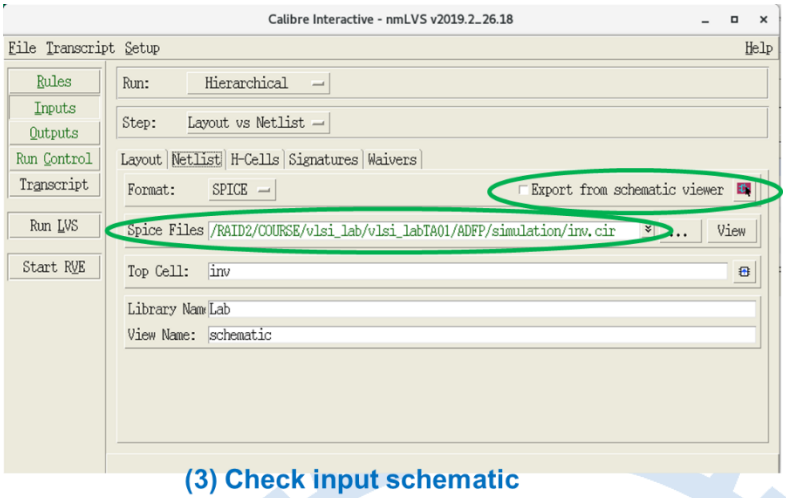
(3)點選「Inputs」→「Layout」→ 勾選「Export from layout viewer」



(2) Check input layout

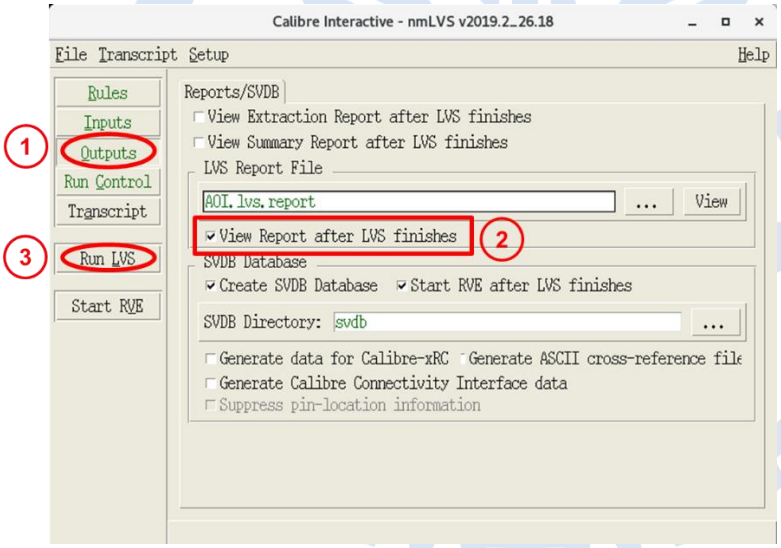
(4)點選「Inputs」→「Netlist」→ 取消勾選「Export from … viewer」

(5)點選「Spice Files 旁的 View」→「選擇 Pre-sim 輸出的 sp 檔案」

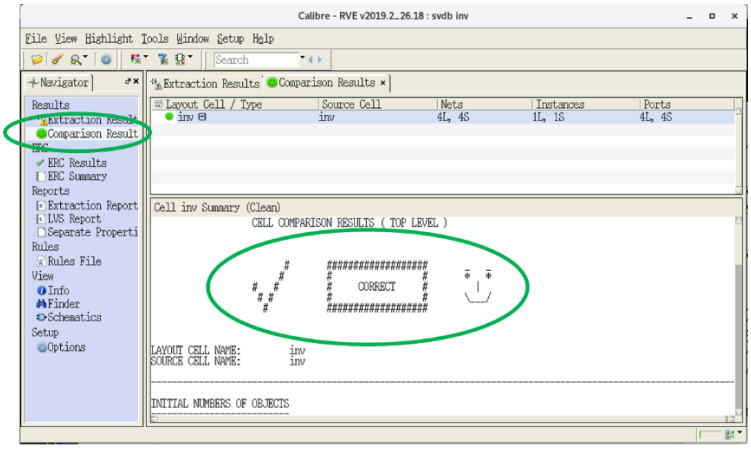


(3) Check input schematic
(Your Pre-Sim Circuit Netlist)

(6)點選「Outputs」→ 勾選「View Report after LVS finishes」→ 「Run LVS」

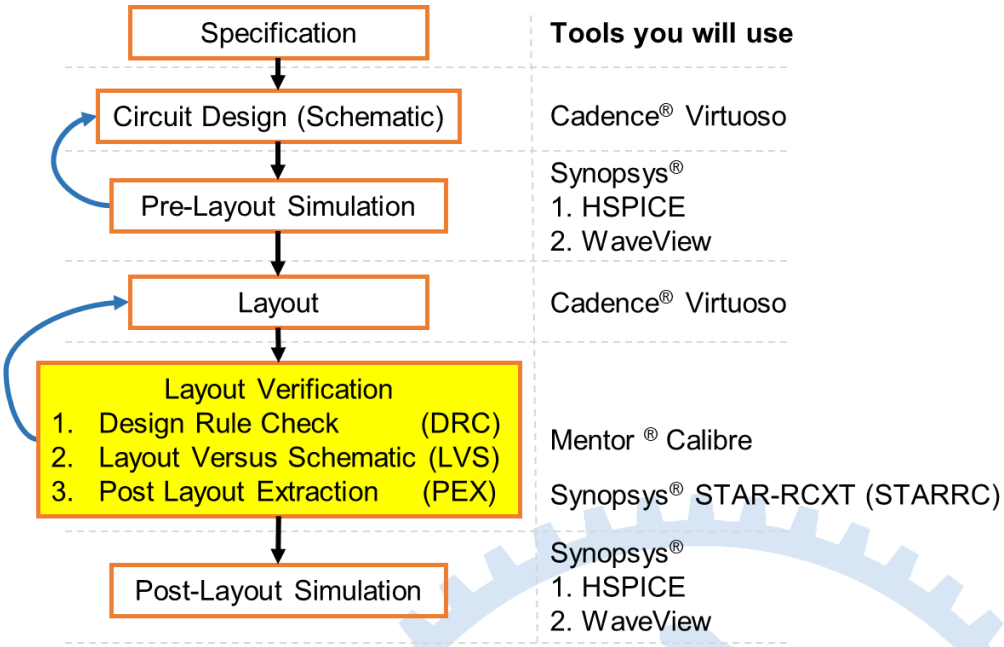


(7)查看 LVS 結果



(5) Check LVS Result

7. Layout Verification – PEX

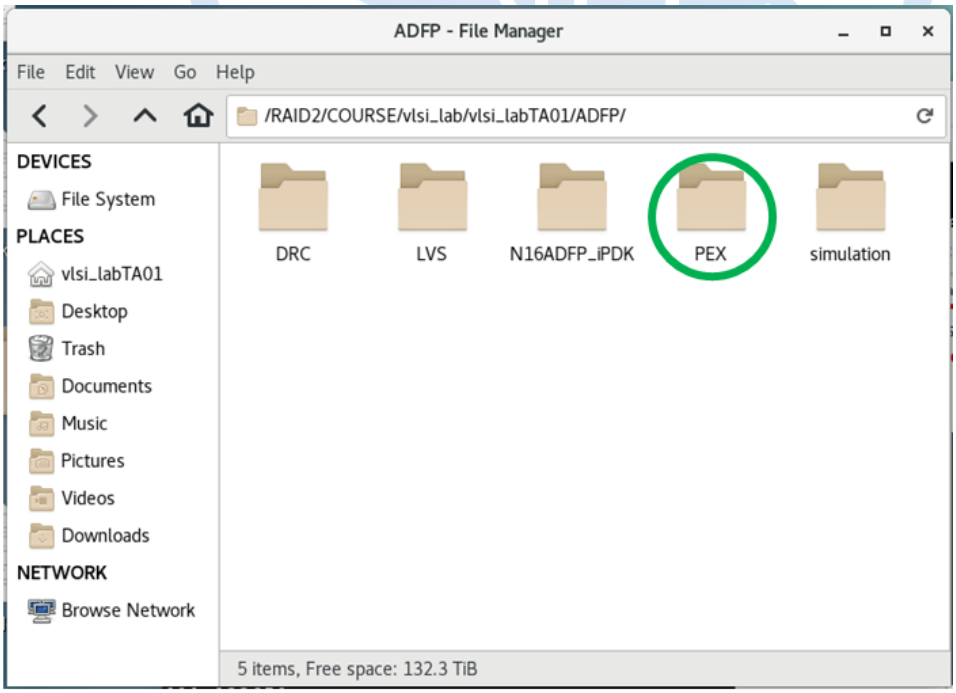


7.1 創建 PEX 資料夾

[~]$ cd ~/ADFP

[~/ADFP]$ mkdir PEX

[~/ADFP]$ cd PEX

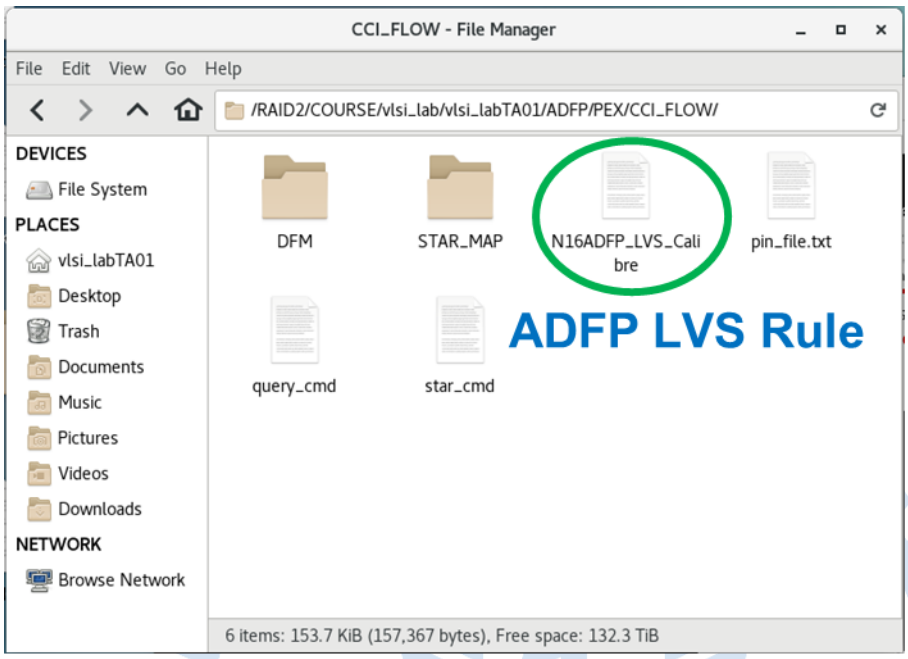


(1) Create new folder for PEX

7.2 拷貝 CCI_Flow 資料夾

[~/ADFP/PEX]$ cp -r /ADFP/Material/CCI_FLOW ./

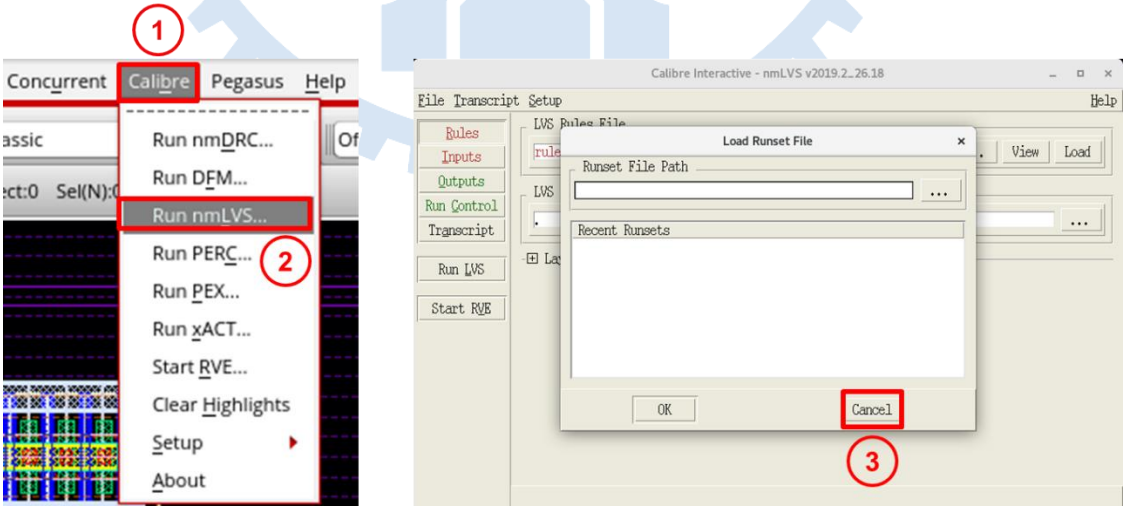
LVS Rule file name: N16ADFP_LVS_Calibre



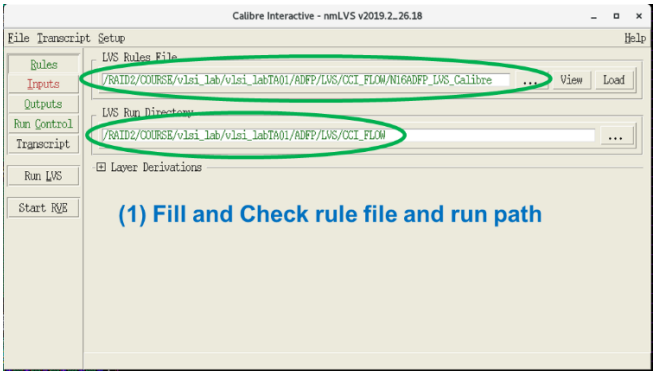
(2) Ensure whole directory is copied

7.3 從 Virtuoso 打開 Calibre LVS，產出 svdb 檔案:

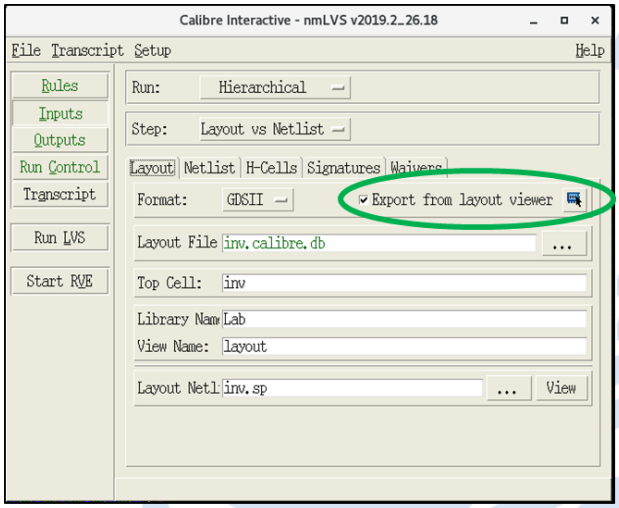
(1)點選「Calibre」→ 「Run nmLVS」→ 「Cancel」



(2)點選「Rules」→「Load」→ 「選取剛剛複製過來的 LVS Rule」



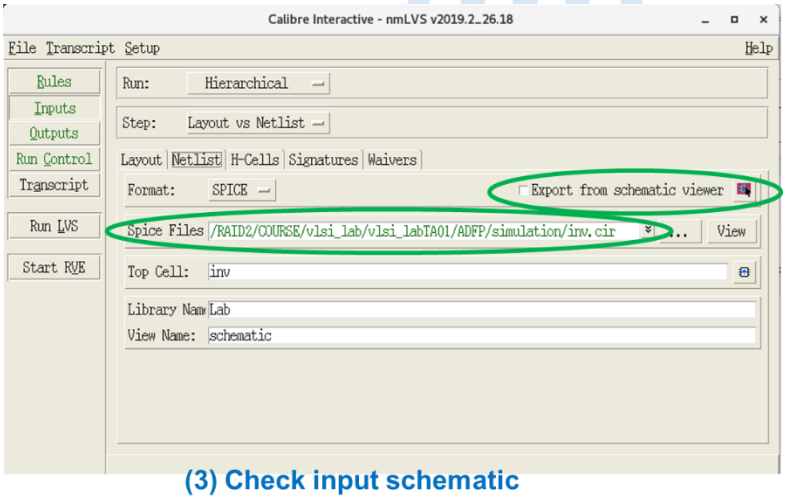
(3)點選「Inputs」→「Layout」→ 勾選「Export from layout viewer」



(2) Check input layout

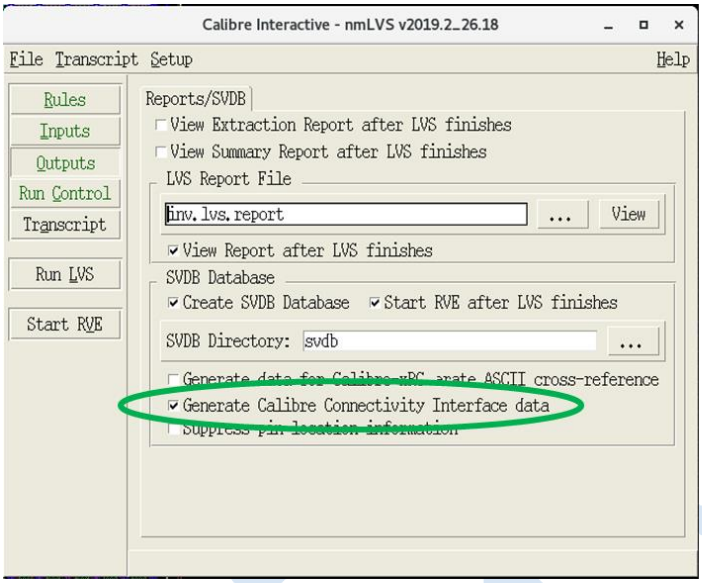
(4)點選「Inputs」→「Netlist」→ 取消勾選「Export from ... viewer」

(5)點選「Spice Files 旁的 View」→「選擇 Pre-sim 輸出的 sp 檔案」



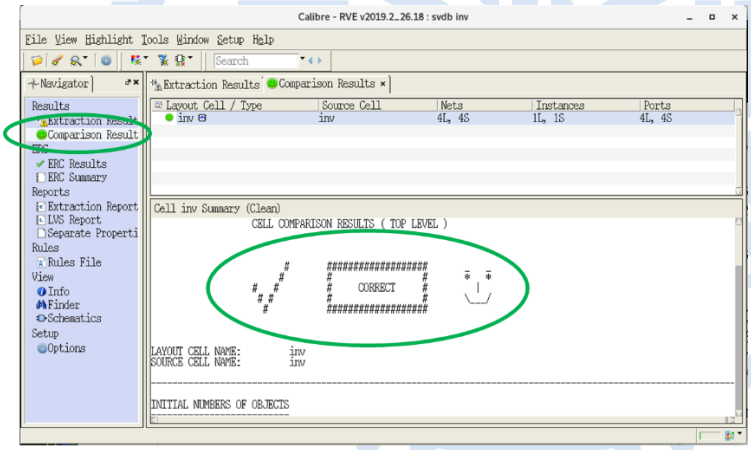
(3) Check input schematic
(Your Pre-Sim Circuit Netlist)

(6)點選「Outputs」→ 勾選「View Report after LVS finishes」→ 勾選「Generate Calibre Connectivity Interface Data」→「Run LVS」



(4) Generate CCI data for STARRC

(7)查看 LVS 結果

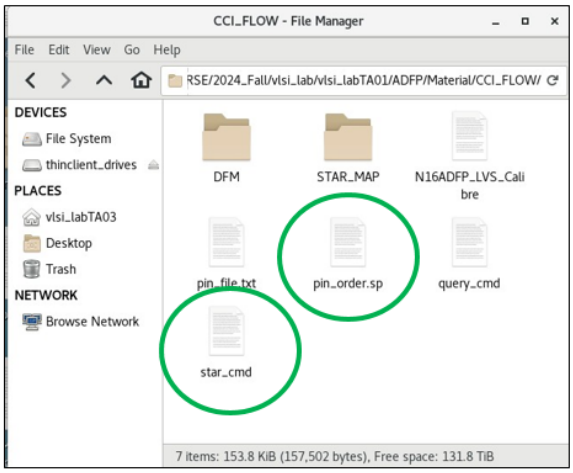


(5) Check LVS Result

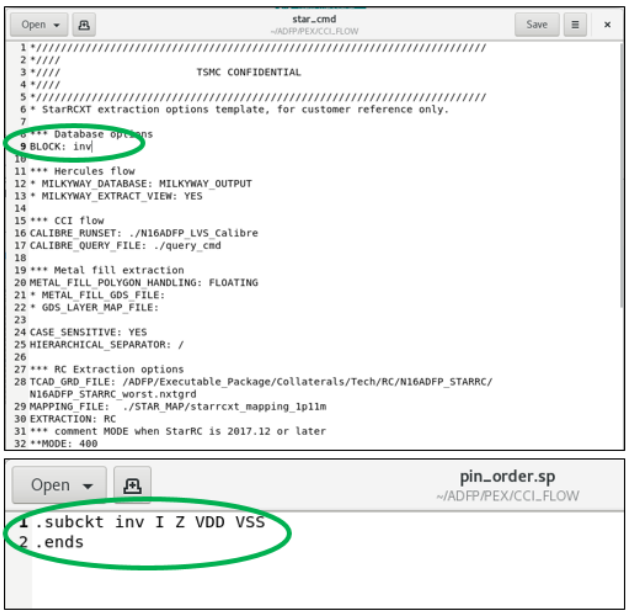
7.4 使用 query_cmd 將 LVS 輸出檔轉為 StarRC 所需輸入檔

[~/ADFP/PEX/CCI_FLOW]$ calibre -query ./svdb/ < query_cmd

7.5 針對欲抽取電路更改 star_cmd 與 pin_order.sp 內容



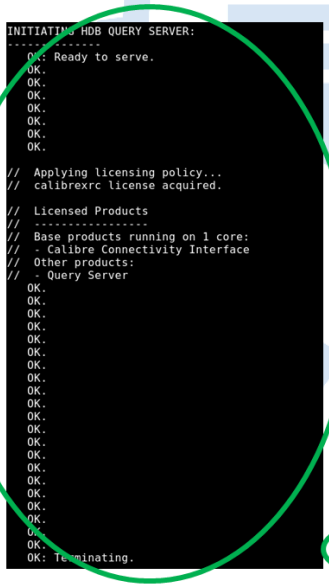
Modify "star_cmd" and "pin_order.sp"



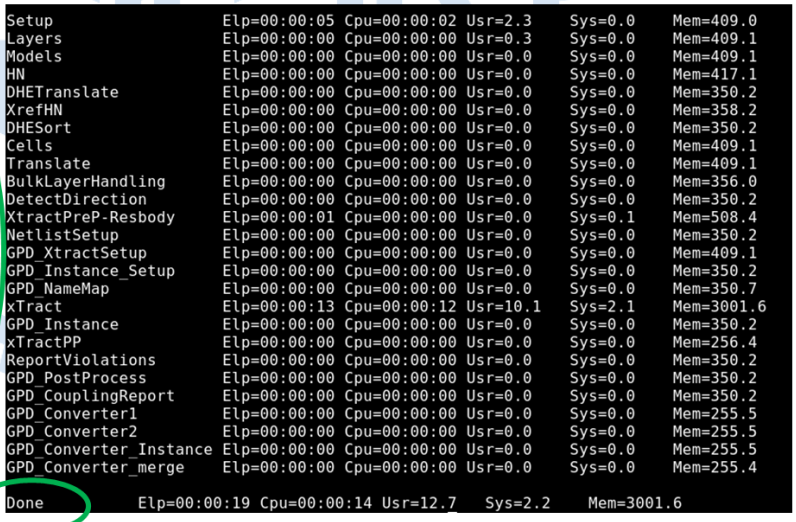
Change Top Cell Name and Sub-Circuit Definition

7.6 根據 star_cmd 內容抽取寄生電路

[~/ADFP/PEX/CCI_FLOW]$ StarXtract -clean star_cmd

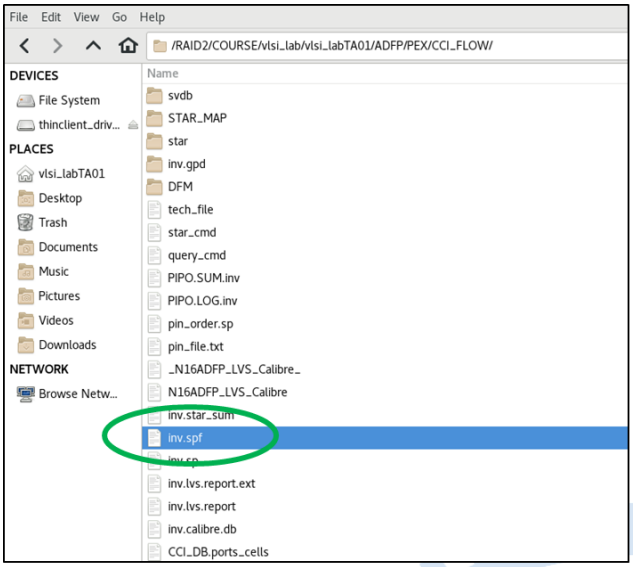


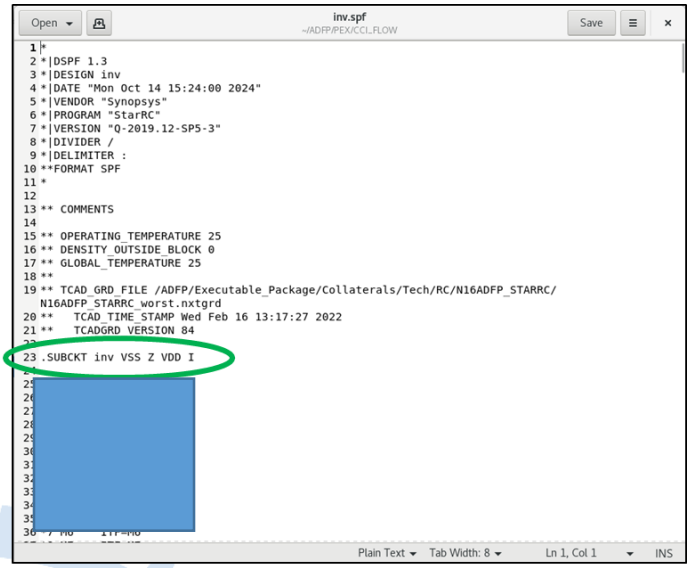
Query Result



Star-RC Result

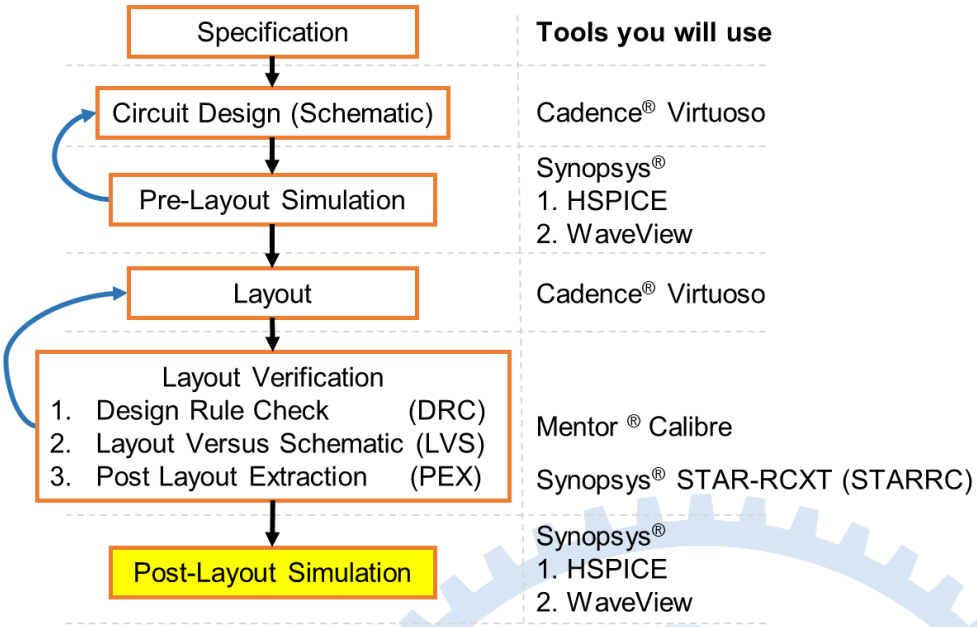
7.7 查看 Extract 出的寄生電路





Extracted Netlist

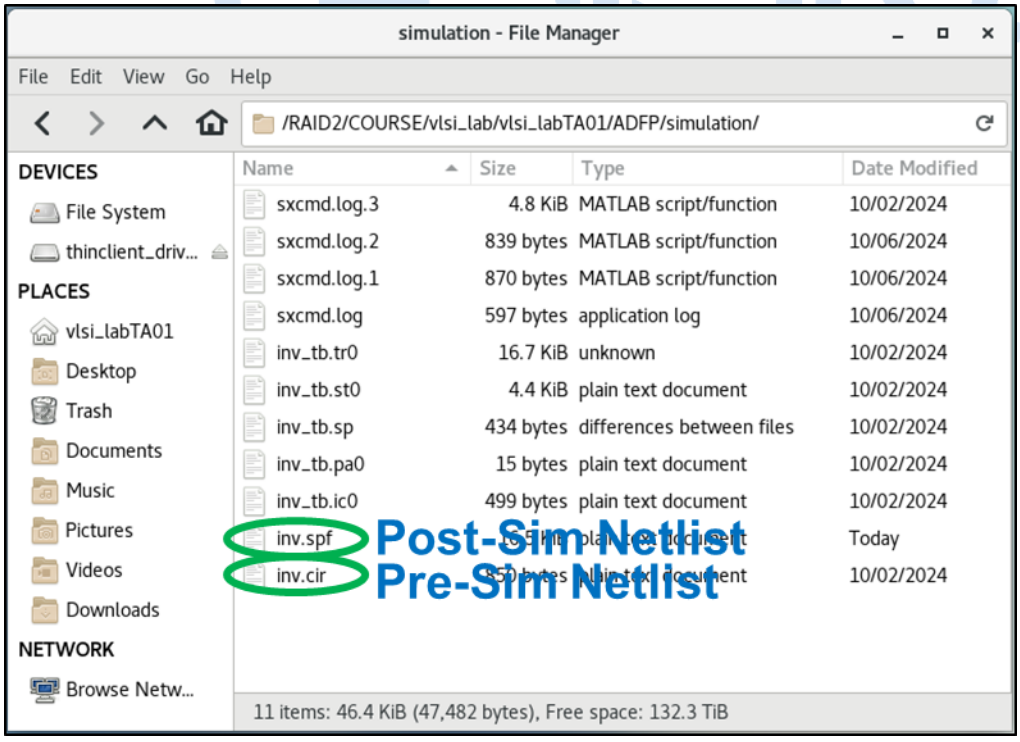
8. Post-Layout Simulation



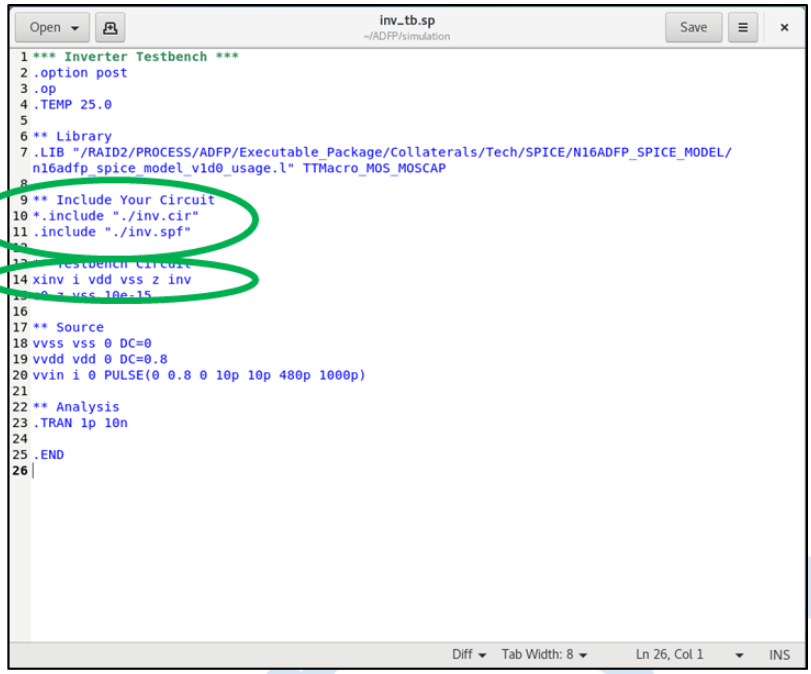
8.1 複製 Layout 產生的 spice 檔案

[~] $ cd ~/ADFP/simulation

[~/ADFP/simulation]$ cp ~/ADFP/PEX/CCI_FLOW/inv.spf ./

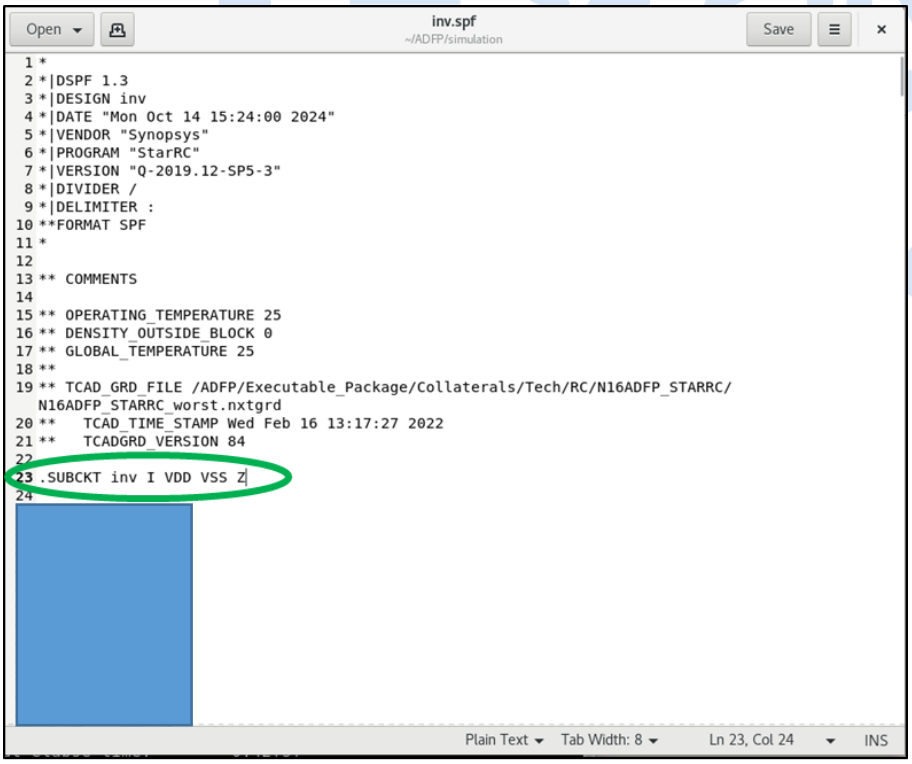


8.2 修改 TestBench include 的 netlist



Modify Testbench Design

8.3 修改並確認 TestBench 呼叫電路時的 Pin 的順序與 netlist 一致



Check Pin Order

8.4 跑 Hspice simulation

[~/ADFP/simulation]$ hspice inv_tb.sp -hpp -mt 4

```
******  Runtime Statistics (seconds)  ******

analysis          time    # points   tot. iter  conv.iter
op point          0.02           1           16
transient         0.05       10001          729         340 rev=        20
readin            0.09
errchk            0.09
setup             0.02
output            0.00


         peak memory used        411.69 megabytes
         total cpu time            0.27 seconds
         total elapsed time        0.44 seconds
         job started at     15:40:07 10/14/2024
         job ended   at     15:40:07 10/14/2024

>info:          ***** hspice job concluded
         job total runtime         0.44 seconds


 lic: Release hspice token(s)
 lic: total license checkout elapse time:        0.17(s)
15:40 vlsi_labTA01@cad11[~/ADFP/simulation]$
```

simulate successfully

當電路比較大時，而為了縮減模擬檔案內容進而節省個人 (組群) 的硬碟空間，請務必於 Hspice Testbench 當中輸入檔中先啟用 .option post=2 probe print 功能，再利用 .probe 或 .print 設定所需要的訊號或資訊即可。

Hspice 電路模擬的補充說明:

為縮減所產生的模擬檔，Hspice 檔案內鍵入 .option post=2 probe print 設定以儲存必要輸出之模樣結果 （最多兩層的結果）。

.OPTION
POST=n Saves results for viewing by an interactive waveform viewer. Default is 0.
PROBE=n Limits post-analysis output to only variables specified in .PROBE and .PRINT statements. Default is 0.

並利用 .probe 與 .print 指令，選取必要輸出的模擬結果，以減少模擬輸出結果檔案大小。

.print test='V (VS) /abs (I (mm1)) '
.probe test='V (VS) /abs (I (mm1)) '
.print 結果會在.list 檔內 （ .lis ） .probe 結果以 waveform （.tr0 ）呈現
.print: Prints numeric analysis results in the output listing file （and post-processor data if .OPTION POST is used ）.
.probe: Outputs data to post-processor output files but not to the output listing （used with .OPTION PROBE to limit output ）.

- 參考資料: HSPICE: Quick Reference | HSPICE: User Guide, Simulation and Analysis | HSPICE: Reference Manual

Hspice 平行運算設定說明:

如果電路龐大可使用平行運算功能，Hspice 提供兩種平行運算機制:

(1)本機單工多緒機制 (-mt，適用單一模擬工作)。

- 在此模式下 Hspice 利用多緒做加速運算，故需 N 個 CPU core。
- 指令範例： **hspice inv_tb.sp -mt N**
- 建議加上參數 hpp (high performance parallel)，效果更好
- 指令範例： **hspice inv_tb.sp -mt N –hpp**

(2)本機多工多緒機制 (-mp 加 -mt，但 overhead 較重)。

- 當使用 ALTER 可拆成多個多緒子工作，共需 N x M 個 CPU core。

  .param supply = 1.8v
  .alter
  .param supply = 2v
  .alter
  .param supply = 1.6v 共需跑三次，此時用-mp 3 會有顯著效果。

- 指令範例：**hspice test.sp -mp M -mt N –hpp**

Hspice 平行運算效益案例 (藍色為使用 alter 共跑 3 次的檔案模擬):

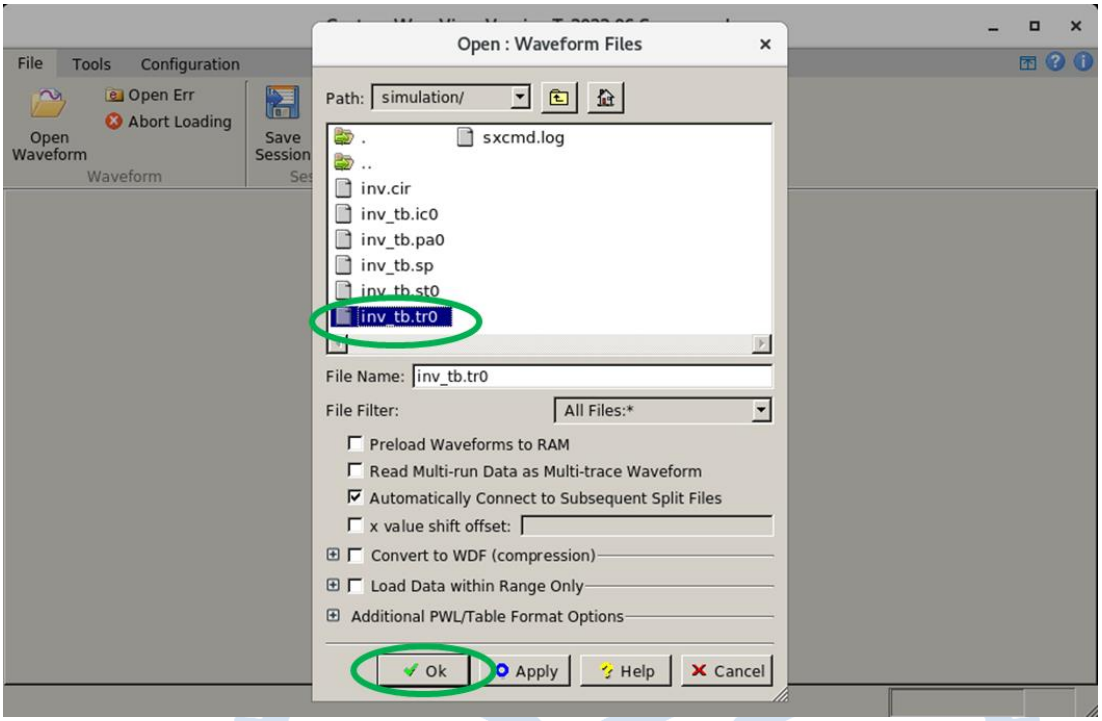
平行運算機制	使用的 core	實際使用率	執行時間	平行運算的效益
無	1	98%	12:03	1 X
-mt 2	2	198%	13:22	0.9 X
-mt 4	4	396%	11:47	1.02 X
-mt 4 -hpp	4	387%	03:52	3.12 X

平行運算機制	使用的 core	實際使用率	執行時間	平行運算的效益
無	1	99%	36:10	1 X
-mt 4 -hpp	4	390%	12:21	2.93 X
-mp 3 -mt 4 -hpp	12	99% (主線程)	04:29	8.07 X

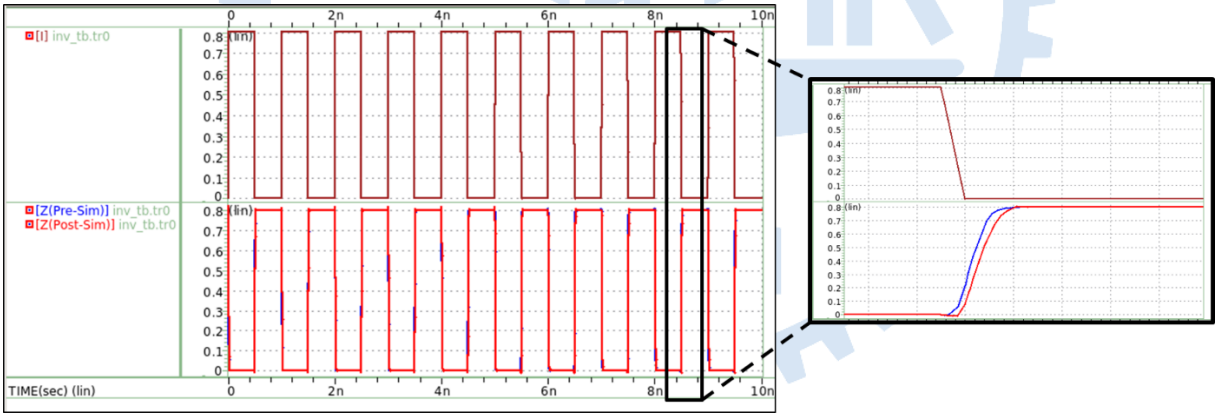
Note: 請盡量不要超過 -mt 4 避免資源的佔用，使用時搭配 -hpp 效果更好。

8.5 使用 WaveView 查看波型

[~/ADFP/simulation]$ wv &



8.6 點擊欲察看訊號，比較 Pre-sim 和 Post-sim 差異。



9. 查看 TSMC 提供之 FC 文件範例練習

請參閱家目錄的浮水印文件，有關 FC 說明:
~/Desktop/ADFP_PDF/

(1) ADFP046_TSMC_N16ADFP_Introduction_20220118_wmc.pdf

有關 TSMC ADFP 製程的簡要說明。

(2) ADFP044_TSMC_N16ADFP_Layout_20220118_wmc.pdf

有關 2D-Planner 和 FinFET Layout 的理論介紹和差異(圖解)

以及特別的 DRC Rule 和 Layer 層說明。

(3) ADFP042_TSMC_N16ADFP_Lab_Layout_20220211_wmc.pdf

該文件提供 Lab 練習，使用 Layout Tool 繪製基本邏輯閘。

(4) ADFP047_TSMC_N16ADFP_SPICE_20220118_wmc.pdf

有關 Spice model 的說明。

10. 查看 NYCU 課程提供之 FC 文件範例練習

請參閱家目錄的浮水印文件，有關 FC 說明:
~/Desktop/ADFP_PDF/

(1) **COURSE04_VLSILAB_ADFP_full_custom_tutorial_2024-01-12.pdf**

有關 TSMC ADFP 製程的簡要說明。有關 2D-Planner 和 FinFET Layout 的理論介紹和差異(圖解)以及特別的 DRC Rule 和 Layer 層說明。

(2) **COURSE05_VLSILAB_ADFP_layout_tutorial_2024-01-12.pdf**

有關如何「善用」ADFP 各層來實現 AOI 數位邏輯閘。

Revision Record and Author List

Original Tutorial by 施品辰、莊勝傑、蕭邦原

2024.11.18 Version 1 edited by Lin-Hung Lai